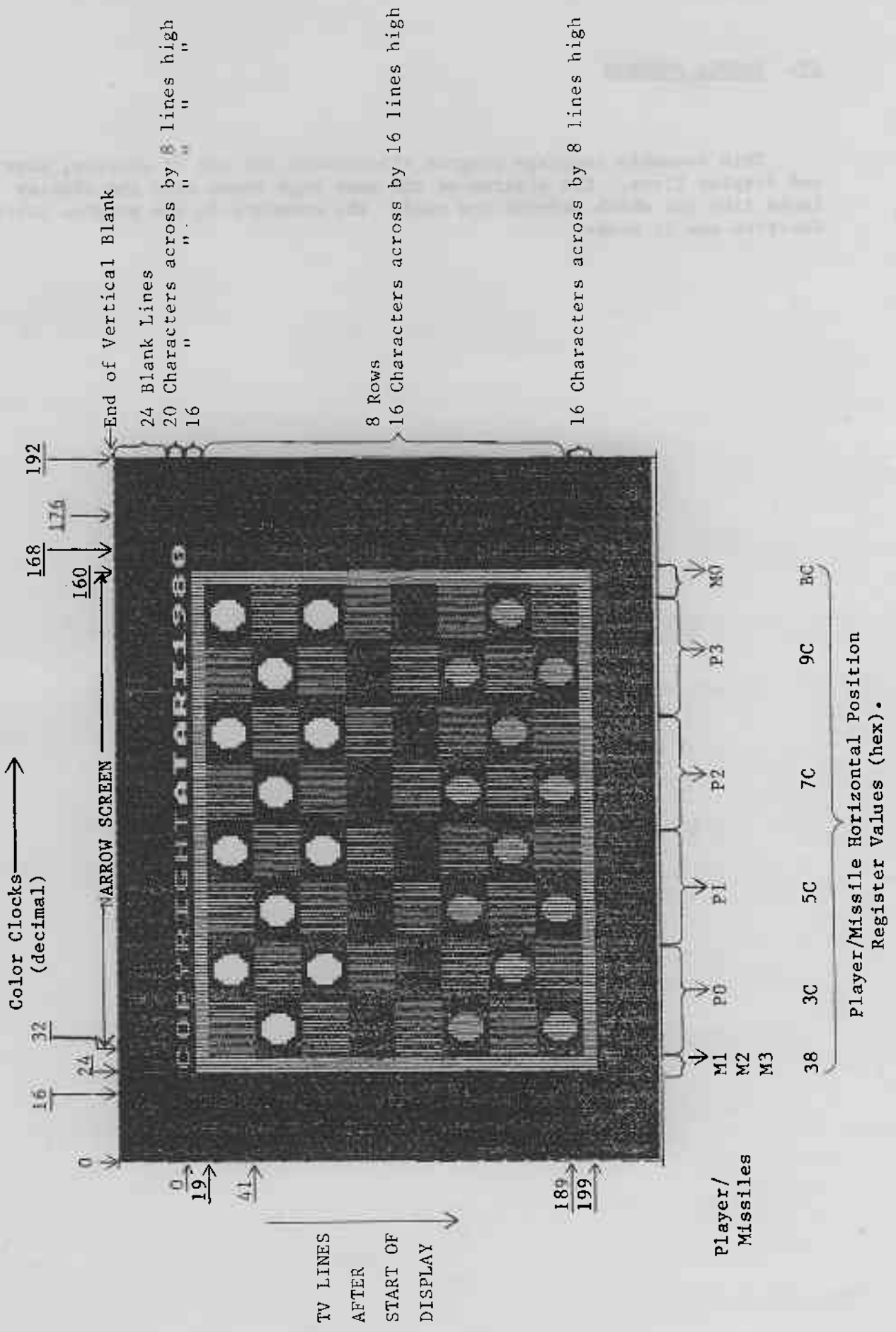


IV. SAMPLE PROGRAM

This assembly language program illustrates the use of players, missiles, and display lists. The diagram on the next page shows what the display looks like and which objects are used. The comments in the program listing describe how it works.



CHECKERS DISPLAY



30 ; COPYRIGHT ATARI 1980
 40 ;
 50 ; THIS IS AN EXAMPLE OF A DISPLAY LIST WHICH USES CHARACTER MAPPING TO
 60 ; PRODUCE THE CHECKERS AND THE TOP AND BOTTOM BORDERS OF THE BOARD.
 70 ; PLAYERS ARE USED FOR THE RED SQUARES. THIS GIVES 6 COLORS WITHOUT
 80 ; CHANGING THE COLOR REGISTERS.
 90 ; MISSILES ARE USED FOR THE LEFT AND RIGHT BORDERS
 100 ; THE PROGRAM STARTS AT THE LOCATION SPECIFIED BY PME.
 110 ; A FEW TRICKS ARE USED TO SAVE RAM, BUT FURTHER OPTIMIZATION IS POSSIBLE
 120 ; THIS IS A RAM BASED PROGRAM WHICH RUNS WITH THE ASSEMBLER CARTRIDGE. NOT A
 130 ; ROM CARTRIDGE.
 140 ;

```

0150 ; COLLEEN (ATARI 800) EQUATES
0160 ;
0170 CHEASE = $D409
0180 DRACTL = $D406
0190 SDMCTL = $D22F
0200 HPOSPO = $D000
0210 SIZEPO = $D008
0220 PCOLRO = $D2C8
0230 SDSLTL = $D230
0240 SDSLTH = $D231
0250 GRACL = $D01D
0260 PMBASE = $D487
0270 GPRIOR = $D26F
0280 VDSLST = $D200
0290 NMIEEN = $D40E
0300 ;
0310 ; DISPLAY LIST EQUATES
0320 ;
0330 INT = $80
0340 JMPWT = $41
0350 RELOD = $40
0360 VSC = $20
0370 HSC = $10
0380 JUMP = 1
0390 BLANK1 = 0
0400 BLANK2 = $10
0410 BLANK3 = $20
0420 BLANK4 = $30
0430 BLANK5 = $40
0440 BLANK6 = $50
0450 BLANK7 = $60
0460 BLANK8 = $70

0080 ; DISPLAY LIST INTERRUPT (BIT 7 OF NMI STATUS)
0041 ; JUMP AND WAIT UNTIL END OF NEXT VERTICAL BLANK (3 BYTES)
0040 ; RELOAD MEM SCAN COUNTER (3 BYTES)
0020 ; VERTICAL SCROLL ENABLE
0010 ; HORIZONTAL SCROLL ENABLE
0001 ; JUMP INSTRUCTION (3 BYTES)
0000 ; 1 BLANK TV LINE
0010 ; 2 BLANK LINES
0020 ; 3
0030 ; 4
0040 ; 5
0050 ; 6
0060 ; 7
0070 ; 8 BLANK TV LINES
    
```


ATARI 800 CHECKERS DISPLAY BY C. SHAW 3/31/88

```

0000      0850      PAGE
0000      0860 ;
0000      0870 ; PAM VARIABLES
0000      0880 ;
0000      0890      **= PNB
0000      5000 BOARD **= **32 ; CHECKER BOARD (ONLY 32 BLACK SQUARES ARE USED)
0000      5020      **= **1 ; TEMP FOR MOVING BOARD TO MEN MAP
0000      0920 ;
0000      0930 ; PLAYER AND MISSILE GRAPHICS
0000      0940 ; PLAYERS ARE USED FOR SQUARES, MISSILES FOR LEFT AND RIGHT BORDERS.
0000      0950 ;
0000      0960      **= PNB+$180
0000      5180 GRM03 **= **$80 ; MISSILE GRAPHICS
0000      5200 GRP0 **= **$80 ; PLAYER 0 GRAPHICS
0000      5280 GRP1 **= **$80 ; PLAYER 1
0000      5300 GRP2 **= **$80 ;
0000      5380 GRP3 **= **$80 ;
0000      1020 ;
0000      5400 TITL **= **20 ; TOP LINE OF CHARS -- ATASCII MESSAGE
0000      5414 TOPBRD **= **16 ; TOP BORDER OF BOARD
0000      5424 BRDSP **= 8*16** ; BOARD DISPLAY
0000      5484 BOTBRD **= **16 ; BOTTOM BORDER

```

ATARI 800 CHECKERS DISPLAY BY C. SHAW 3/31/80

5484	1070	. PAGE
	1080	;
	1090	; GP -- SPECIAL CHECKER'S CHARACTER SET (ONLY CODES 0-4 ARE USED)
	1100	;
	1110	+= PMB+*F00
	1120	GR
	1130	. BYTE 0,0,0,0,0,0,0,0 ; BLANK (0)
5600 00	1140	. BYTE \$3C,\$7E,\$FF,\$FF,\$FF,\$7E,\$3C ; CHECKER (1)
5601 00		
5602 00		
5603 00		
5604 00		
5605 00		
5606 00		
5607 00		
5608 3C		
5609 7E		
560A FF		
560B FF		
560C FF		
560D FF		
560E 7E		
560F 3C		
5610 3C	1150	. BYTE \$3C,\$7E,\$F5,\$F5,\$C3,\$C3,\$7E,\$3C ; KING (2)
5611 7E		
5612 A5		
5613 A5		
5614 C3		
5615 C3		
5616 7E		
5617 3C		
5618 C3	1160	. BYTE \$C3,\$66,\$3C,\$18,\$18,\$3C,\$66,\$C3 ; CURSOR (3)
5619 66		
561A 3C		
561B 18		
561C 18		
561D 3C		
561E 66		
561F C3		
5620 00		
5621 FF		
5622 FF	1170	. BYTE 0,\$FF,\$FF,\$FF,\$FF,\$FF,\$FF,\$FF ; BORDER (4)
5623 FF		
5624 FF		
5625 FF		
5626 FF		
5627 00		

ATARI 800 CHECKERS DISPLAY BY C. SHAW 3/31/80

```

5628 70      1180      PAGE
5629 70      1190
562A 70      1200      DISPLAY LIST
562B 46      1210
562C 0054    1220
562E 80      1230      DSP
562F 06      1248      BYTE BLANKS ; 24 BLANK LINES
5630 10      1250      BYTE BLANKS
5631 07      1260      BYTE RELOAD*6 ; LINES 0-7. MESSAGE LINE: 20 ACROSS X 5 COLOR X 1 LINE RESOLUTION CHARACTERS
5632 50      1270      WORD TITL ; 9-16. TOP BORDER: 16 X 5 X 1 CHARS (LAST LINE IS TOP OF 1ST ROW OF SQUARES)
5633 07      1280      BYTE INT+BLANK1 ; B. INTERRUPT TO CHANGE CHARACTER BASE ADDRESS AND CHANGE TO NARROW SCREEN
5634 50      1290      BYTE BLANK2 ; 17-18. TOP OF FIRST ROW OF SQUARES
5635 07      1300      BYTE BLANK2 ; 19-34. 16X5X2 LINE RESOLUTION CHARS
5636 50      1310      BYTE 7 ; 35-40. FIRST 3 LINES=TOP OF PREVIOUS SQUARE.
5637 07      1320      BYTE BLANKS ; 41-56
5638 50      1330      BYTE BLANKS ; 57-62. LAST 3 LINES=TOP OF NEXT SQUARE.
5639 07      1340      BYTE BLANKS ; 63-78
563A 50      1350      BYTE 7 ; 79-84
563B 07      1360      BYTE BLANKS ; 85-100
563C 50      1370      BYTE BLANKS ; 101-106
563D 07      1380      BYTE BLANKS ; 107-122
563E 50      1390      BYTE BLANKS ; 123-128
563F 07      1400      BYTE BLANKS ; 129-144
5640 50      1410      BYTE BLANKS ; 145-150
5641 06      1420      BYTE 7 ; 151-166
5642 41      1430      BYTE BLANK6 ; 167-172
5643 2856    1440      BYTE 7 ; 173-188
5644 10      1480      NEXT THREE LINES ARE BOTTOM OF PREVIOUS SQUARE.
5645 06      1490      BYTE BLANK2 ; 189-190. END OF NORMAL DISPLAY (SHOULD BE ON SCREEN ON ALL TV'S).
5646 41      1500      BYTE 6 ; 191-198. BOTTOM BORDER (MAY OVERSCAN, BUT NOT ESSENTIAL TO GAME PLAY)
5647 2856    1510      BYTE JMPWIT ; WAIT FOR NEXT VBLANK, THEN START OVER
5648 808004  1520      WORD DSP
5649 808004  1530
564A 808004  1540
564B A92D    1550      DSP -- DISPLAY LIST INTERRUPT HANDLER.
564C 808004  1560      CHANGES CHARACTER BASE AND WIDTH OF DISPLAY FOR SPECIAL CHECKERS GRAPHICS.
564D 808004  1570      THE 05 WILL CHANGE CHBASE BACK TO NORMAL DURING VERTICAL BLANK.
564E 808004  1580
564F 808004  1590      NCHR
5650 68      1600      PHR
5651 40      1610      LDA #GR/256
5652 40      1620      STA CHBASE
5653 40      1630
5654 40      1640      INSTRUCTION FETCH DMA ENABLE. P/M 2 LINE RES. P/M DMA ENABLE. NARROW SCREEN (128 CLOCKS)
5655 40      1650      LDA #12D
5656 40      1660      STA DMACTL
5657 40      1670      PLA
5658 40      1680      RTI

```

ATARI 800 CHECKERS DISPLAY BY C. SHAW 3/31/80

```

5652      1690 ; PAGE
1700 ;
1710 ; INITIALIZATION CODE -- START EXECUTION HERE
1720 ;
1730 ; ** PMB+$700
1740 ;
1750 ; INIT OS'S DMACTL VARIABLE
1760 ; INSTRUCTION FETCH DMA ENABLE, P/M 2 LINE RES, P/M DMA ENABLE, STANDARD SCREEN (160 CLOCKS)
1770 ;
5700 A92E 1780 LDA #*2E
5702 8D2F02 1790 STA SOMCTL
1800 ;
1810 ; CLEAR RAM
1820 ;
5705 A900 1830 LDA #0
5707 AA 1840 TAX
1850 ;
5708 9D0050 1860 STA PMB,X
570B 9D0051 1870 STA PMB+$100,X
570E 9D0052 1880 STA PMB+$200,X
5711 9D0053 1890 STA PMB+$300,X
5714 9D0054 1900 STA PMB+$400,X
5717 E8 1910 INX
5718 D0EE 1920 BNE INITLP
1930 ;
1940 ; INITIALIZE MISSILE GRAPHICS FOR BORDERS
1950 ;
571A A90E 1960 LDA #*0E
571C A05E 1970 LDY #*5E
571E 999451 1980 LOPZ STA GRM03+$14,Y
5721 88 1990 DEY
5722 D0FA 2000 BNE LOPZ
2010 ;
2020 ; INITIALIZE TOP AND BOTTOM BORDERS
2030 ;
5724 A010 2040 LDY #16
5726 A9C4 2050 LDA #CLBOR+BORDER
5728 991354 2060 TBLP STA TOPBRD-1,Y
572B 99A354 2070 STA BOTBRD-1,Y
572E 88 2080 DEY
572F D0F7 2090 BNE TBLP ; CONTINUE UNTIL Y=0
2100 ;
2110 ; INITIALIZE PLAYER GRAPHICS FOR SQUARES (CHECKER BOARD) Y=0
2120 ;
5731 A9F0 2130 LDA #*F0
5733 A20A 2140 LDX #10
5735 991852 2150 IN2 STA GRP0+$18,Y
5738 999852 2160 IN3 STA GRP1+$18,Y
573B 991853 2170 STA GRP2+$18,Y
573E 999853 2180 STA GRP3+$18,Y
2190 ;

```


ATARI 800 CHECKERS DISPLAY BY C. SHAW 3/31/80

```

5741 48      2200      PHR
5742 A90A    2210      LDA #A0A
5744 999851 2220      STA GRM03+*10.Y ; REST OF MISSILE GRAPHICS
5747 68      2230      PLA
5748 C8      2240      INV
5749 CA      2250      DEX
574A 10E9    2260      BPL IN3
574C 43FF    2270      EOR #3FF ; FILL IN OPPOSITE SQUARES
574E C058    2280      COPY #38
5750 90E1    2290      BCC IN2
5752 A008    2300      LDY #3
5753        2310 ;
5754        2320 ; INITIALIZE PLAYER AND MISSILE POSITIONS AND COLORS
5755        2330 ;
5756        2340 IN4
5757 990000 2350      STA HPOS0.Y ; #FF
5758 8A      2360      TXA
5759 990800 2370      STA SIZE0.Y ; #03 INDICATES 4 TIMES NORMAL SIZE (REST IS DON'T CARE)
575B B9E057 2380      LDA ITBL1.Y
575D 99C002 2390      STA PCOL0.Y
575E 88      2400      DEY
575F 10ED    2410      BPL IN4
5760        2420 ;
5761        2430 ; OS, ANTIC, POKEY INITIALIZATION
5762        2440 ;
5763        2450
5764 A928    2450      LDA #DSP&#FF ; DISPLAY LIST START ADDRESS (LSB)
5765 803002 2460      STA SDLSTL
5766 A956    2470      LDA #DSP/256 ; MSB OF ADDRESS
5767 803102 2480      STA SDLSTH
5768 A903    2490      LDA #3
5769 801D00 2500      STA GRACL
576A A950    2510      LDA #PMB/256 ; MSB OF ADDRESS OF PLAYER/MISSILE GRAPHICS
576B 800704 2520      STA PMBASE
576C A914    2530      LDA #14 ; 5TH PLAYER ENABLE (USE PF3 FOR MISSILE COLOR), PF TAKES PRIO OVER PLAYERS
576D 806F02 2540      STA GPRIDR ; OS PRIORITY REG
576E A945    2550      LDA #NCHR&#FF ; DISPLAY LIST INTERRUPT VECTOR (LSB)
576F 800002 2560      STA VDSLST
5770 A956    2570      LDA #NCHR/256
5771 800102 2580      STA VDSLST+1
5772 8E0ED4 2590      STX NMEN ; X=#FF #C0 ENABLES DISPLAY LIST & VBLANK INTERRUPTS.
5773        2600 ;
5774        2610 ; INITIALIZE BOARD DISPLAY
5775        2620 ;
5776        2630
5777 A20B    2630      LDX #11
5778 A901    2640      LDA #CHECKER+CLP0 ; HUMAN PIECES ON SQUARES 0-11
5779 900050 2650      STA BOARD.X
577A A981    2660      LDA #CHECKER+CLP1 ; COMPUTER PIECES ON SQUARES 20-31
577B 9D1450 2670      STA BOARD+20.X
577C CA      2680      DEY
577D 10F3    2690      BPL BRDLP
577E        2700
577F        2710
5780        2720
5781        2730
5782        2740
5783        2750
5784        2760
5785        2770
5786        2780
5787        2790
5788        2800
5789        2810
5790        2820
5791        2830
5792        2840
5793        2850
5794        2860
5795        2870
5796        2880
5797        2890
5798        2900
5799        2910
5800        2920
5801        2930
5802        2940
5803        2950
5804        2960
5805        2970
5806        2980
5807        2990
5808        3000
5809        3010
5810        3020
5811        3030
5812        3040
5813        3050
5814        3060
5815        3070
5816        3080
5817        3090
5818        3100
5819        3110
5820        3120
5821        3130
5822        3140
5823        3150
5824        3160
5825        3170
5826        3180
5827        3190
5828        3200
5829        3210
5830        3220
5831        3230
5832        3240
5833        3250
5834        3260
5835        3270
5836        3280
5837        3290
5838        3300
5839        3310
5840        3320
5841        3330
5842        3340
5843        3350
5844        3360
5845        3370
5846        3380
5847        3390
5848        3400
5849        3410
5850        3420
5851        3430
5852        3440
5853        3450
5854        3460
5855        3470
5856        3480
5857        3490
5858        3500
5859        3510
5860        3520
5861        3530
5862        3540
5863        3550
5864        3560
5865        3570
5866        3580
5867        3590
5868        3600
5869        3610
5870        3620
5871        3630
5872        3640
5873        3650
5874        3660
5875        3670
5876        3680
5877        3690
5878        3700
5879        3710
5880        3720
5881        3730
5882        3740
5883        3750
5884        3760
5885        3770
5886        3780
5887        3790
5888        3800
5889        3810
5890        3820
5891        3830
5892        3840
5893        3850
5894        3860
5895        3870
5896        3880
5897        3890
5898        3900
5899        3910
5900        3920
5901        3930
5902        3940
5903        3950
5904        3960
5905        3970
5906        3980
5907        3990
5908        4000
5909        4010
5910        4020
5911        4030
5912        4040
5913        4050
5914        4060
5915        4070
5916        4080
5917        4090
5918        4100
5919        4110
5920        4120
5921        4130
5922        4140
5923        4150
5924        4160
5925        4170
5926        4180
5927        4190
5928        4200
5929        4210
5930        4220
5931        4230
5932        4240
5933        4250
5934        4260
5935        4270
5936        4280
5937        4290
5938        4300
5939        4310
5940        4320
5941        4330
5942        4340
5943        4350
5944        4360
5945        4370
5946        4380
5947        4390
5948        4400
5949        4410
5950        4420
5951        4430
5952        4440
5953        4450
5954        4460
5955        4470
5956        4480
5957        4490
5958        4500
5959        4510
5960        4520
5961        4530
5962        4540
5963        4550
5964        4560
5965        4570
5966        4580
5967        4590
5968        4600
5969        4610
5970        4620
5971        4630
5972        4640
5973        4650
5974        4660
5975        4670
5976        4680
5977        4690
5978        4700
5979        4710
5980        4720
5981        4730
5982        4740
5983        4750
5984        4760
5985        4770
5986        4780
5987        4790
5988        4800
5989        4810
5990        4820
5991        4830
5992        4840
5993        4850
5994        4860
5995        4870
5996        4880
5997        4890
5998        4900
5999        4910
6000        4920

```

ATARI 800 CHECKERS DISPLAY BY C. SHAW 3/31/80

```

2720 ; MOVE COPYRIGHT MESSAGE TO MESSAGE DISPLAY LINE
2730 ;
579C A213 LDX #19
579E 8DE957 LDA COPY,X
57A1 900854 STA TITL,X
57A4 CR DEX
57A5 10F7 BPL IN6
2790 ;
2800 ; LOOP TO MOVE BOARD TO GRAPHICS AREA
2810 ; THE CHECKERS PROGRAM LOGIC COULD BE ADDED HERE OR A VBLANK INTERRUPT COULD BE USED.
2820 ;
2830 LOOP
57A7 20AD57 JSR UPCHR
57AA 4CA757 JMP LOOP
2860 ;
2870 ;
2880 ;
2890 ;
2900 ;
2910 ;
2920 ;
2930 ;
2940 ;
2950 ;
2960 ;
2970 ;
2980 ;
2990 ;
3000 ;
3010 ;
3020 ;
3030 ;
3040 ;
3050 ;
3060 ;
3070 ;
3080 ;
3090 ;
3100 ;
3110 ;
3120 ;
3130 ;
3140 ;
3150 ;
3160 ;
3170 ;
3180 ;
3190 ;
3200 ;
3210 ;
3220 ;
3230 ;
57AD A21F LDX #31 ; SQUARE 31 = UPPER LEFT
57AF A000 LDY #0
57B1 A903 LDA #4-1 ; 4 SQUARES/LINE
57B3 8D2050 STA T0
57B6 8D0050 LDA BOARD,X
57B9 992654 STA BRDSP+2,Y ; FOR ROWS SHIFTED TO RIGHT
57BC 8DFC4F LDA BOARD-4,X
57BF 953454 STA BRDSP+10,Y ; FOR ROWS SHIFTED TO LEFT
57C2 C8 INY
57C3 C8 INY
57C4 C8 INY
57C5 C8 INY
57C6 CA DEX
57C7 CE2050 DEC T0
57CA 10ER BPL UPLP2
57CC 98 TYA
57CD 18 CLC
57CE 6910 ADC #310
57D0 A8 TAY
57D1 8A TXA
57D2 E903 SEC
57D4 AA TAX
57D5 80DA BCS UPLP1
57D7 60 RTS
; CARRY IS CLEAR (SUBTRACT 4)

```

ATARI 800 CHECKERS DISPLAY BY C. SHAW 3/31/80

3240 ; DATA
 3250 ; HORIZONTAL POSITION OF PLAYERS (SQUARES) AND MISSILES (SIDE BORDERS).
 3260 ; M0-FIGHT BORDER, M1-LEFT BORDER
 3270 ; M2 & M3 ARE PLACED WITH M1.
 ; P0, P1, P2, P3, M0, M1, M2, M3
 3290 ITBL
 3300 . BYTE \$3C, \$5C, \$7C, \$9C, \$BC, \$38, \$38, \$38

5708 3C
 5709 5C
 57DA 7C
 57DB 9C
 57DC BC
 57DD 38
 57DE 38
 57DF 38

3310 ; COLOR TABLE
 3320 ; COLOR TABLE
 3330 ITBL1
 3340 . BYTE \$34, \$34, \$34, \$34 ; 4 PLAYERS (RED SQUARES)

57E0 34
 57E1 34
 57E2 34
 57E3 34
 57E4 36
 57E5 88
 57E6 0E
 57E7 26
 57E8 00

3350 . BYTE \$36 ; PF0: RED CHECKERS AND MESSAGES
 3360 . BYTE \$88 ; PF1: BLUE CHARACTERS
 3370 . BYTE \$0E ; PF2: WHITE CHECKERS AND MESSAGES
 3380 . BYTE \$26 ; PF3: YELLOW BORDER (CHARS & MISSILES)
 3390 . BYTE 0 ; BK: BLACK BACKGROUND
 3400 ;
 3410 ; "COPYRIGHT ATARI 1980" MESSAGE
 3420 ;

0000
 0080
 0040

3430 0F = \$00 ; FOR PF0 COLOR (RED)
 3440 0F2 = \$80 ; FOR PF2 COLOR (WHITE)
 3450 0F3 = \$40 ; FOR PF1 COLOR (BLUE)
 3460 ITBL

57E9 00
 57EA 23
 57EB 2F
 57EC 30
 57ED 39
 57EE 32
 57EF 29
 57F0 27
 57F1 28
 57F2 34
 57F3 A1
 57F4 B4
 57F5 A1
 57F6 B2
 57F7 A9
 57F8 51
 57F9 59
 57FA 58
 57FB 50

3470 COPY . BYTE SPI, CI+OF, OI+OF, PI+OF, VI+OF, RI+OF, II+OF, GI+OF, HI+OF, TI+OF

3480 . BYTE AI+OF2, II+OF2, AI+OF2, RI+OF2, II+OF2, NI+OF3, N9I+OF3, N8I+OF3, N0I+OF3

V. HARDWARE REGISTER LISTS

A. ADDRESS ORDER

CTIA ADDRESSES								
Address	WRITE		READ					
	Name	Description	Name	Description				
D0FF	REPEAT AS BELOW		7 MORE TIMES					
D020								
D01F					CONSOL	Write Consol SW.Port	CONSOL	Read Consol SW. Port
D01E					HITCLR	Collision Clear		
D01D					GRCTL	Graphic Control		
D01C					VDELAY	Vert. Delay		
D01B					PRIOR	Priority Select		
D01A					COLBK	Col-lum Bkgnd		
D019	COLPF3	Color-lum of 3						
D018	COLPF2	Playfield 2						
D017	COLPF1	Playfield 1						
D016	COLPF0	Playfield 0						
D015	COLPM3	Color-lum of 3						
D014	COLPM2	Player-Missile 2	PAL	READ PAL/NTSC bits				
D013	COLPM1	Player-Missile 1	TRIG3	Read Joystick				
D012	COLPM0	Player-Missile 0	TRIG2	Trigger				
D011	GRAFM	Graphics All Missiles	TRIG1	Buttons				
D010	GRAFP3	Graphics Player 3	TRIG0					
D00F	GRAFP2	Graphics Player 2	P3PL	Read Player				
D00E	GRAFP1	Graphics Player 1	P2PL	to Player				
D00D	GRAFP0	Graphics Player 0	P1PL	Collisions				
D00C	SIZEM	Size All Missiles	POPL					
D00B	SIZEP3	Size Player 3	M3PL	Read Missile				
D00A	SIZEP2	Size Player 2	M2PL	To Player				
D009	SIZEP1	Size Player 1	M1PL	Collisions				
D008	SIZEP0	Size Player 0	MOPL					
D007	HPOSM3	Horz. Posit. Missile 3	P3PF	Read Player				
D006	HPOSM2	Horz. Posit. Missile 2	P2PF	To Playfield				
D005	HPOSM1	Horz. Posit. Missile 1	P1PF	Collisions				
D004	HPOSM0	Horz. Posit. Missile 0	P0PF					
D003	HPOSP3	Horz. Posit. Player 3	M3PF	Read Missile				
D002	HPOSP2	Horz. Posit. Player 2	M2PF	To Playfield				
D001	HPOSP1	Horz. Posit. Player 1	M1PF	Collisions				
D000	HPOSP0	Horz. Posit. Player 0	M0PF					

ANTIC ADDRESSES

Address	WRITE		READ	
	Name	Description	Name	Description
D4FF ↕ D410	} REPEAT (AS BELOW)		15 MORE TIMES	
D40F	NMIRE5	Reset NMI Interrupt Status NMI Interrupt	NMIST	NMI Interrupt Status Register
D40E	NMIEN	ENABLE		
D40D			PENV	Light Pen Register Vertical
D40C			PENH	Light Pen Register Horizontal
D40B			VCOUNT	Vertical Line Counter
D40A	WSYNC	Wait for HBLANK Synchronism		
D409	CHBASE	Character Base Address Red		
D408				
D407	PMBASE	Player-Missile Base Address Register		
D406				
D405	VSCROL	Vertical Scroll Register		
D404	HSCROL	Horizontal Scroll Register		
D403	DLISTH	Display List Pointer (High Byte)		
D402	DLISTL	Display List Pointer (Low Byte)		
D401	CHACTL	Character Control Register		
D400	DMACTL	DMA Control Register		

POKEY ADDRESSES

	WRITE		READ	
	Name	Description	Name	Description
D2FF ↕ D210	} REPEAT (AS BELOW)		15 MORE TIMES	
D20F	SKCTLS	Serial Port 4 Key Control	SKSTAT	Serial Port 4 Key Status Register
D20E	IRQEN	IRQ Interrupt Enable	IRQST	IRQ Interrupt Status Register
D20D	SEROUT	Serial Port Output Reg.		Serial Port Input Register
D20C				
D20B	POTGO	Start Pot Scan Sequence		Vertical Line
D20A	SKRES	Reset Status (SKSTAT)	RANDOM	Random Numb Generator
D209	STIMER	Start Timers	KBCODE	Keyboard Code
D208	AUDCTL	Audio Control	ALLPOT	Read 8 Line Pot Port State
D207	AUDC4	Audio Channel 4 Control	POT 7	Read the value of each POT
D206	AUDF4	Audio Channel 4 Frequency	POT 6	
D205	AUDC3	Audio Channel 4 Control	POT 5	
D204	AUDF3	Audio Channel 3 Frequency	POT 4	
D203	AUDC2	Audio Channel 2 Control	POT 3	
D202	AUDF2	Audio Channel 2 Frequency	POT 2	
D201	AUDC1	Audio Channel 1 Control	POT 1	
D200	AUDF1	Audio Channel 1 Frequency	POT 0	

PIA ADDRESSES

Address	WRITE		READ	
	Name	Description	Name	Description
D3FF	Repeat as shown below many times			
D304				
D303	PBCTL	PORT B CONTROL	PBCTL	Same as write
D302	PACTL	PORT A CONTROL	PACTL	Same as write
D301	PORTB	Direction Register If PBCTL Bit 2=0 (otherwise)	PORTB	Same as write
	PORTB	Jack 2 & Jack 3 If Direction Bits Are 1 *	PORTB	Jack 2 & Jack 3 If Direction Bits Are 0 *
D300	PORTA	Direction Register If PACTL Bit 2=0 (Otherwise)	PORTA	Same as write
	PORTA	Jack 0 & Jack 1 If Direction Bits Are 1 *	PORTA	Jack 0 & Jack 1 If Direction Bits Are 0 *

* NOTE: Output data is retained in Jack Output Registers.
If direction bits are true, a read of the jacks
will read old data from these registers.

B. ALPHABETICAL ORDER

Hardware Register				OS Shadow		
Name	Description	Address		Name	Address	
		Hex	Dec		Hex	Dec
ALLPOT	Read 8 line Pot Port State	D208	53768			
AUDC1	Audio Channel 1 Control	D201	53761			
AUDC2	Audio Channel 2 Control	D203	53763			
AUDC3	Audio Channel 3 Control	D205	53765			
AUDC4	Audio Channel 4 Control	D207	53767			
AUDCTL	Audio Control	D208	53768			
AUDF1	Audio Channel 1 Frequency	D200	53760			
AUDF2	Audio Channel 2 Frequency	D202	53762			
AUDF3	Audio Channel 3 Frequency	D204	53764			
AUDF4	Audio Channel 4 Frequency	D206	53766			
CHACTL	Character Control	D401	54273	CHART	2F3	755
CHBASE	Character base address	D409	54281	CHBAS	2F4	756
COLBK	Color-Luminance of Background	D01A	53274	COLOR4	2C8	712
COLPF0	Color Luminance of Playfield 0	D016	53270	COLOR0	2C4	708
COLPF1	Color Luminance of Playfield 1	D017	53271	COLOR1	2C5	709
COLPF2	Color Luminance of Playfield 2	D018	53272	COLOR2	2C6	710
COLPF3	Color Luminance of Playfield 3	D019	53273	COLOR3	2C7	711
COLPM0	Color Luminance of Player-Missile 0	D012	53266	PCOLR0	2C0	704
COLPM1	Color Luminance of Player-Missile 1	D013	53267	PCOLR1	2C1	705
COLPM2	Color Luminance of Player-Missile 2	D014	53268	PCOLR2	2C2	706
COLPM3	Color Luminance of Player-Missile 3	D015	53269	PCOLR3	2C3	707
CONSOL	Console Switch Port	D01F	53279	Set to 8 during VBLANK		
DLISTH	Display List Pointer (high byte)	D403	54275	SDLSTH	231	561
DLISTL	Display List Pointer (low byte)	D402	54274	SDLSTL	230	560
DMACTL	Direct Memory Access (DMA) Control	D400	54272	SDMCTL	22F	559
GRACTL	Graphic Control	D01D	53277			
GRAFM	Graphics for all Missiles	D011	53265			
GRAFP0	Graphics for Player 0	D00D	53261			
GRAFP1	Graphics for Player 1	D00E	53262			
GRAFP2	Graphics for Player 2	D00F	53263			
GRAFP3	Graphics for Player 3	D010	53264			
HITCLR	Collision Clear	D01E	53278			
HPOSM0	Horizontal Position of Missile 0	D004	53252			
HPOSM1	Horizontal Position of Missile 1	D005	53253			
HPOSM2	Horizontal Position of Missile 2	D006	53254			
HPOSM3	Horizontal Position of Missile 3	D007	53255			
HPOSP0	Horizontal Position of Player 0	D000	53248			
HPOSP1	Horizontal Position of Player 1	D001	53249			
HPOSP2	Horizontal Position of Player 2	D002	53250			
HPOSP3	Horizontal Position of Player 3	D003	53251			
HSCROL	Horizontal Scroll	D404	54276			
IRQEN	Interrupt Request (IRQ) Enable	D20E	53774	POKMSK	10	16
IRQST	IRQ Status	D20E	53774			
KBCODE	Keyboard Code	D209	53769	GH	2FC	764
MOPF	Missile 0 to Playfield Collisions	D000	53248			
MOPL	Missile 0 to Player Collisions	D008	53256			
M1PF	Missile 1 to Playfield Collisions	D001	53249			
M1PL	Missile 1 to Player Collisions	D009	53257			
M2PF	Missile 2 to Playfield Collisions	D002	53250			
M2PL	Missile 2 to Player Collisions	D00A	53258			

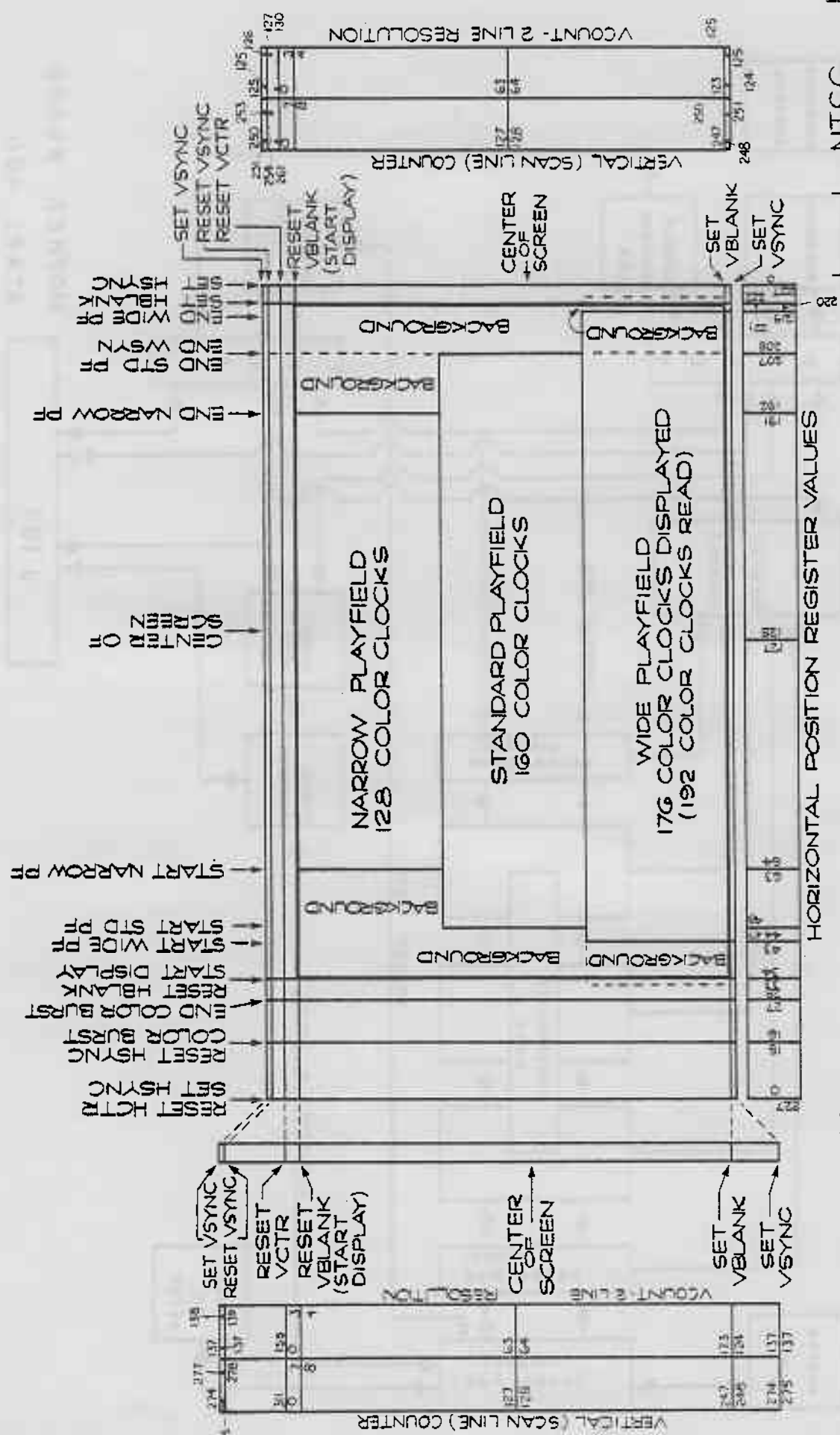
Hardware Register				OS Shadow		
Name	Description	Address		Name	Address	
		Hex	Dec		Hex	Dec
M3PF	Missile 3 to Playfield Collisions	D003	53251			
M3PL	Missile 3 to Player	D00B	53259			
NMIEN	Non-Maskable Interrupt (NMI) Enable	D40E	54286	Set to \$40 by IRQ code written to by NMI code read by NMI code		
NMIRES	NMI reset	D40F	54287			
NMIST	NMI Status	D40F	54287			
POPF	Player 0 to Playfield Collisions	D004	53252			
POPL	Player 0 to Player Collisions	D00C	53260			
P1PF	Player 1 to Playfield Collisions	D005	53253			
P1PL	Player 1 to Player Collisions	D00D	53261			
P2PF	Player 2 to Playfield Collisions	D006	53254			
P2PL	Player 2 to Player Collisions	D00E	53262			
P3PF	Player 3 to Playfield Collisions	D007	53255			
P3PL	Player 3 to Player Collisions	D00F	53263			
PACTL	Port A Control	D302	54018	Set to \$3C by IRQ Code		
PAL	PAL/NTSC indicator	D014	53268			
PBCTL	Port B Control	D303	54019	Set to \$3C by IRQ Code		
PENH	Light Pen Horizontal Position	D40C	54284		LPENH	234
PENV	Light Pen Vertical Position	D40D	54285	LPENV	235	565
PMBASE	Player Missile Base Address	D407	54279			
PORTA	Port A	D300	54016	STICK0,1	278,279	632,633
PORTB	Port A	D301	54017	STICK2,3	27A,27B	634,635
POT0	Pot 0	D200	53760	PADDL0	270,	624
POT1	Pot 1	D201	53761	PADDL1	271	625
POT2	Pot 2	D202	53762	PADDL2	272	626
POT3	Pot 3	D203	53763	PADDL3	273	627
POT4	Pot 4	D204	53764	PADDL4	274	628
POT5	Pot 5	D205	53765	PADDL5	275	629
POT6	Pot 6	D206	53766	PADDL6	276	630
POT7	Pot 7 (right paddle controller)	D207	53767	PADDL7	277	631
POTGO	Start POT Scan Sequence	D20B	53771	WRITTEN DURING VBLANK		
PRIOR	Priority Select	D01B	53275	GPRIOR	26F	623
RANDOM	Random number generator	D20A	53770			
SERIN	Serial Port Input	D20E	53774			
SEROUT	Serial Port output	D20D	53773			
SIZEM	Sizes for all missiles	D00C	53260			
SIZEP0	Size of Player 0	D008	53256			
SIZEP1	Size of Player 1	D009	53257			
SIZEP2	Size of Player 2	D00A	53258			
SIZEP3	Size of Player 3	D00B	53259			
SKCTL	Serial Port Control	D20F	53775	SSKCTL	232	562
SKREST	Reset Serial Port Status (SKSTAT)	D20A	53770			
SKSTAT	Serial Port Status	D20F	53775			
STIMER	Start Timer	D209	53769			
TRIG0	Joystick Controller Trigger 0	D010	53264	STRIG0	284	644
TRIG1	Joystick Controller Trigger 1	D011	53265	STRIG1	285	645
TRIG2	Joystick Controller Trigger 2	D012	53266	STRIG2	286	646
TRIG3T	Joystick Controller Trigger 3	D013	53267	STRIG3	287	647
VCOUNT	Vertical Line Counter	D40B	54283			
VDELAY	Vertical Delay	D01C	54276			
VSCROL	Vertical Scroll	D405	54277			
WSYNC	Wait for Horizontal Sync	D40A	54282	Used by keyboard click routine		

VI. FIGURES

A. MEMORY MAP

ADDRESS	FUNCTION	SIZE
FFFF	Operating System And Math Routines	10K
D800		
D000-D7FF	Hardware Addresses	2K
CFFF	Reserved for Future O.S. expansion	4K
BFFF	ROM Cartridge (Colleen left and right slot and Candy single slot all address to this space)	16K
8000		
7FFF		
	RAM Expansion *	
2000		
1FFF	RAM initially supplied in the product	8K

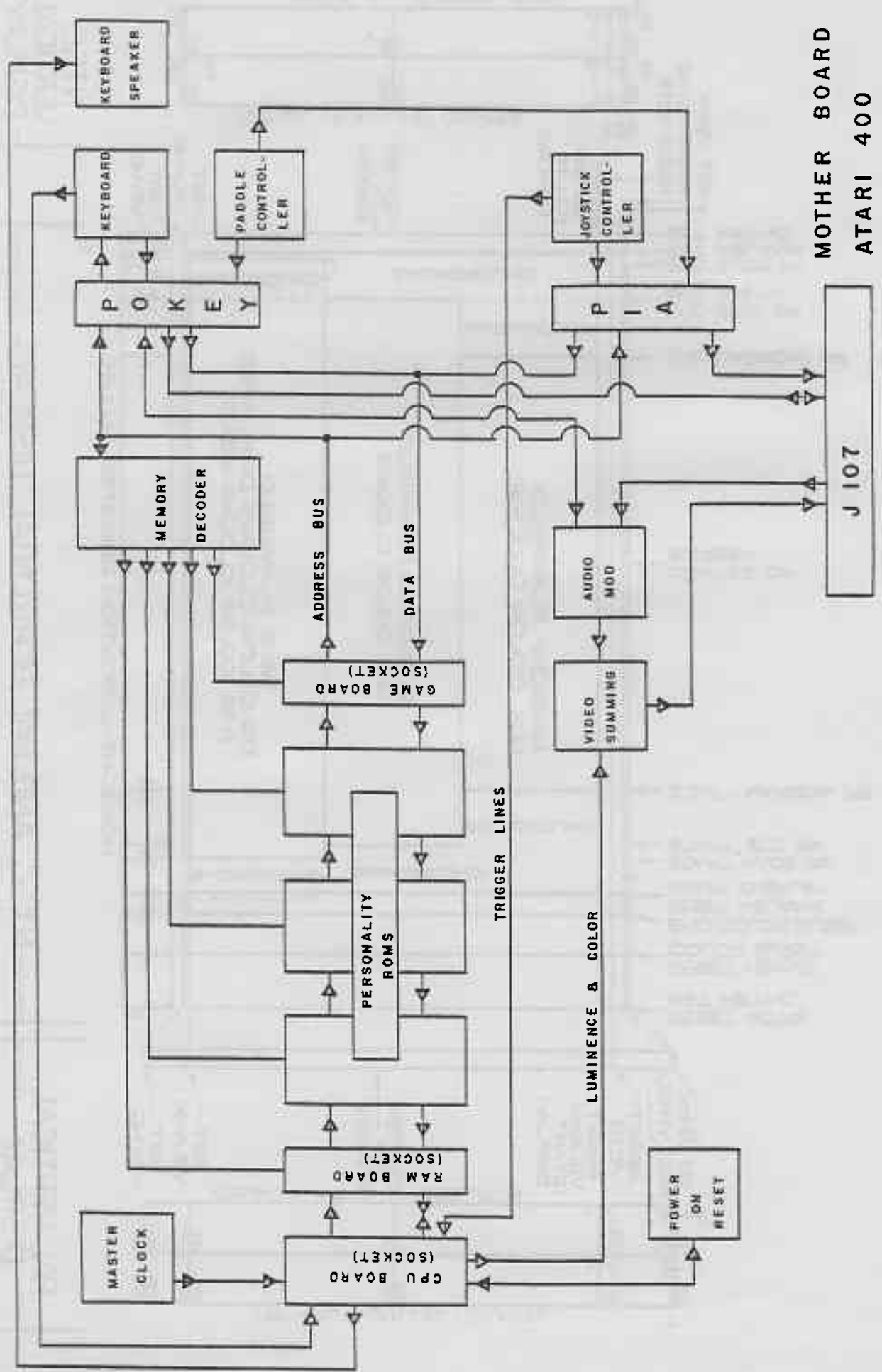
- * RAM expansion can actually extend to BFFF. However, the ROM cartridges will deselect the RAM. Deselection occurs on 8K boundaries. Atari 400 units are RAM expandable only at the factory. They can accept RAM up to 2FFF (16K) when fully extended.



PAL VERTICAL DISPLAY

NTSC AND PAL HORIZONTAL DISPLAY

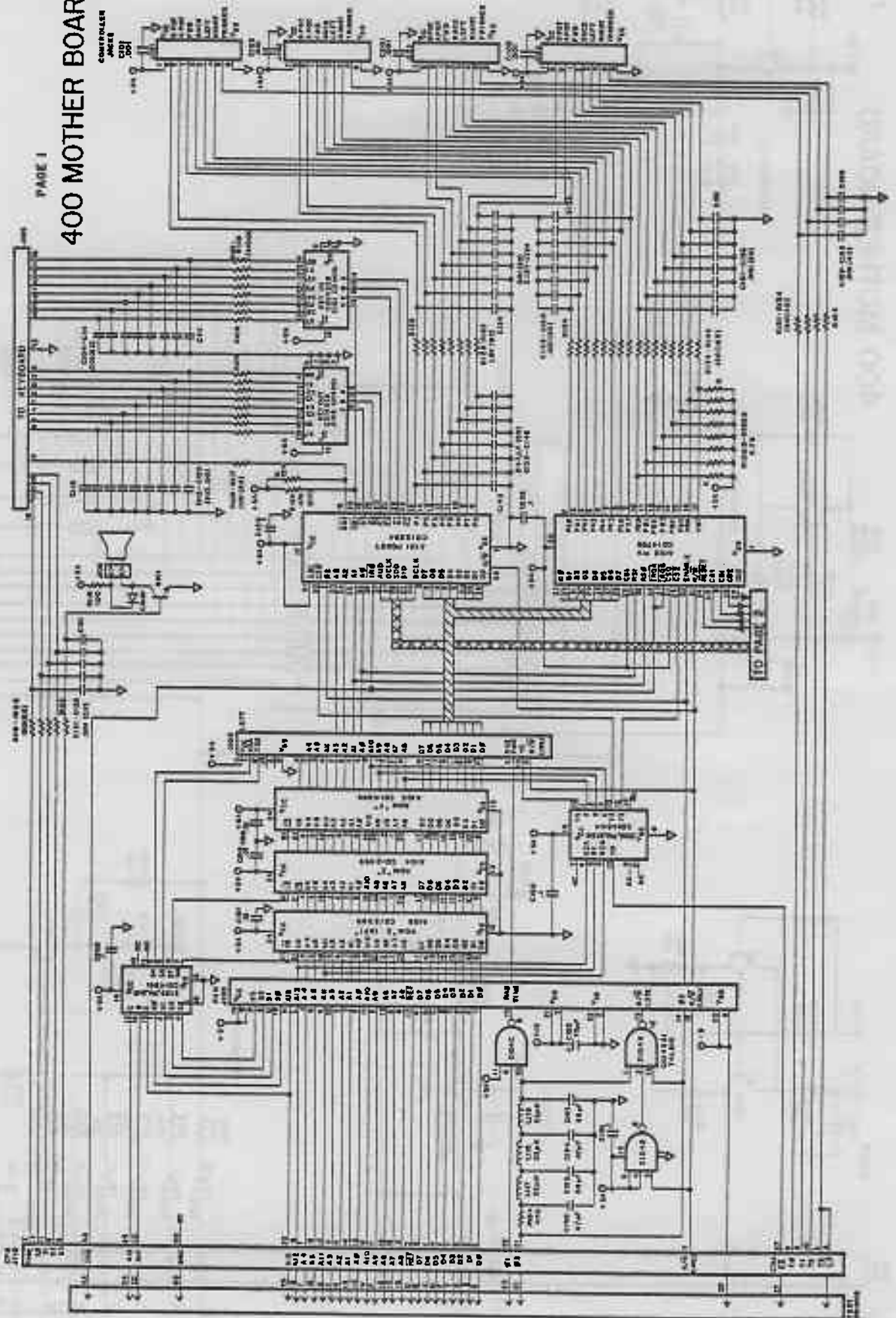
NTSC VERTICAL DISPLAY

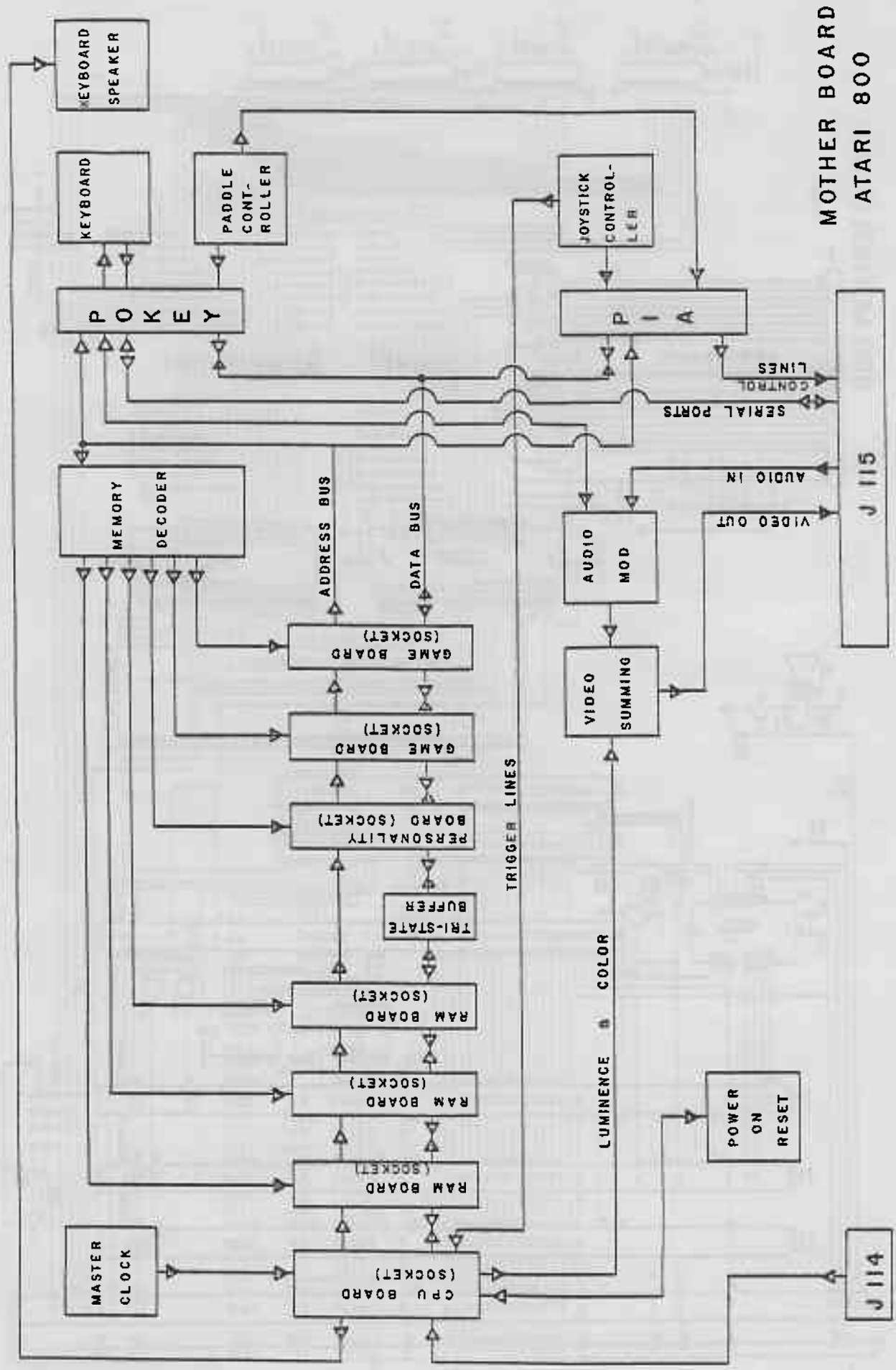


MOTHER BOARD
ATARI 400

400 MOTHER BOARD

CONTROLLER
CIRCUIT
CPU

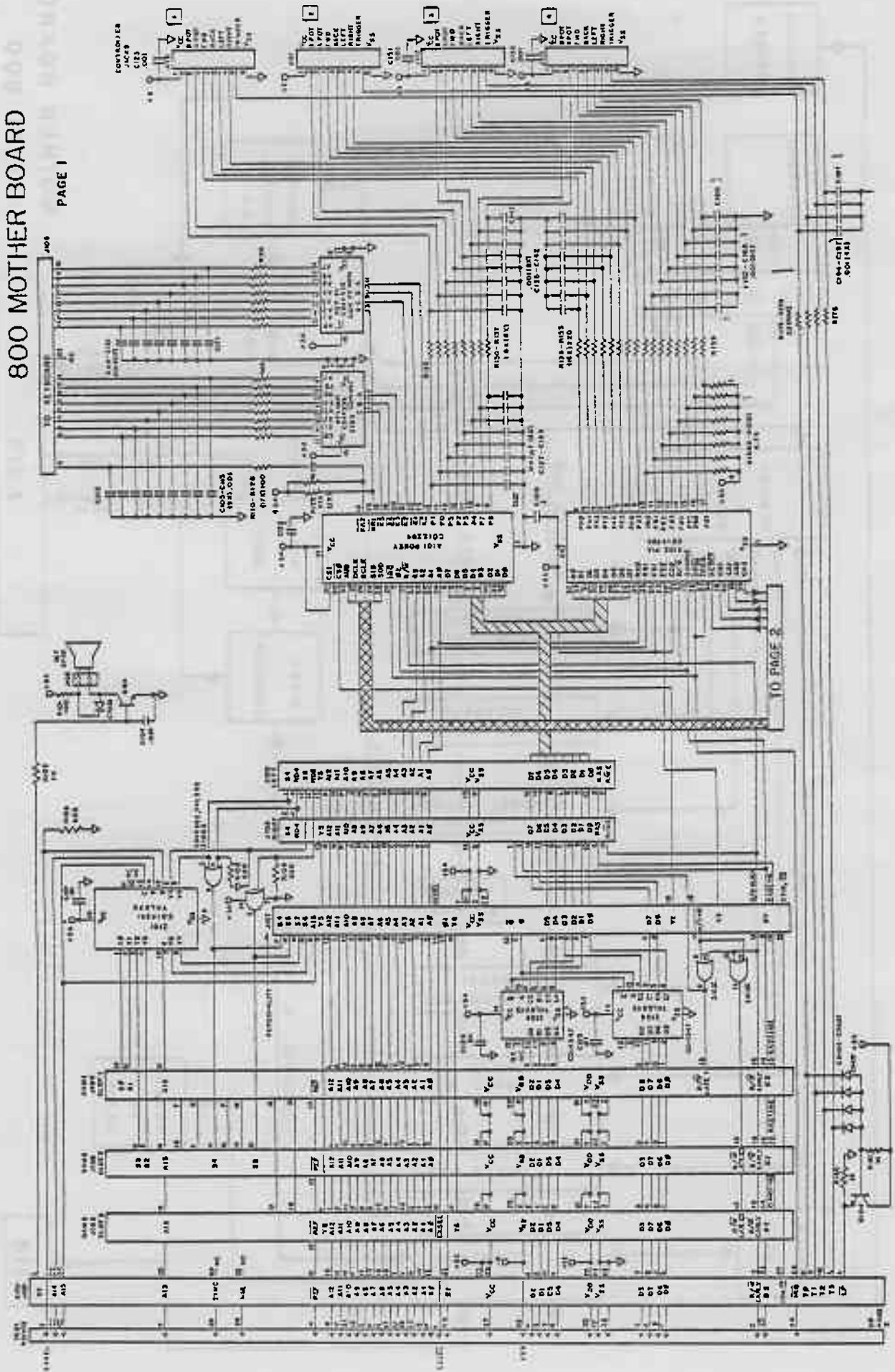




MOTHER BOARD
ATARI 800

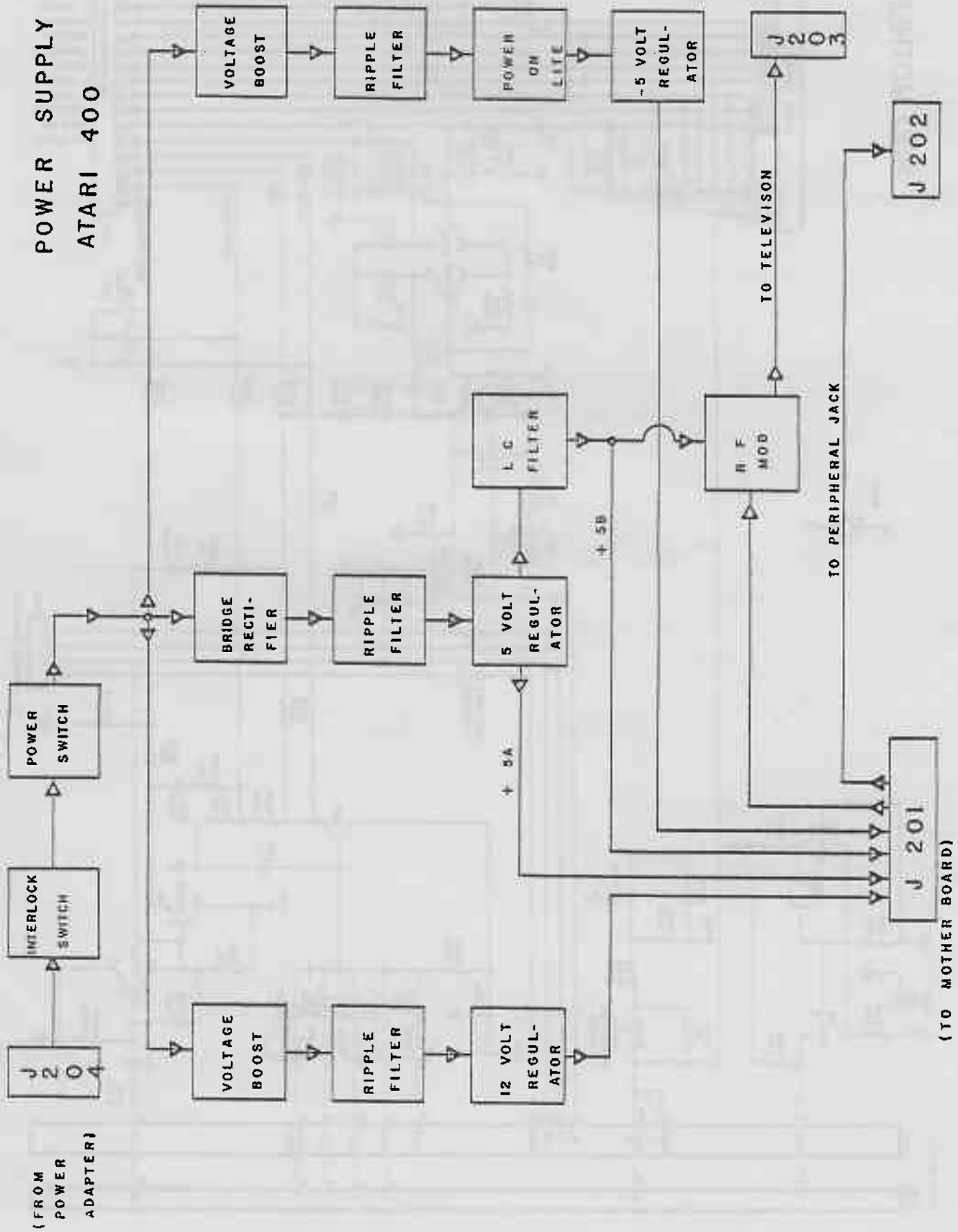
800 MOTHER BOARD

PAGE 1

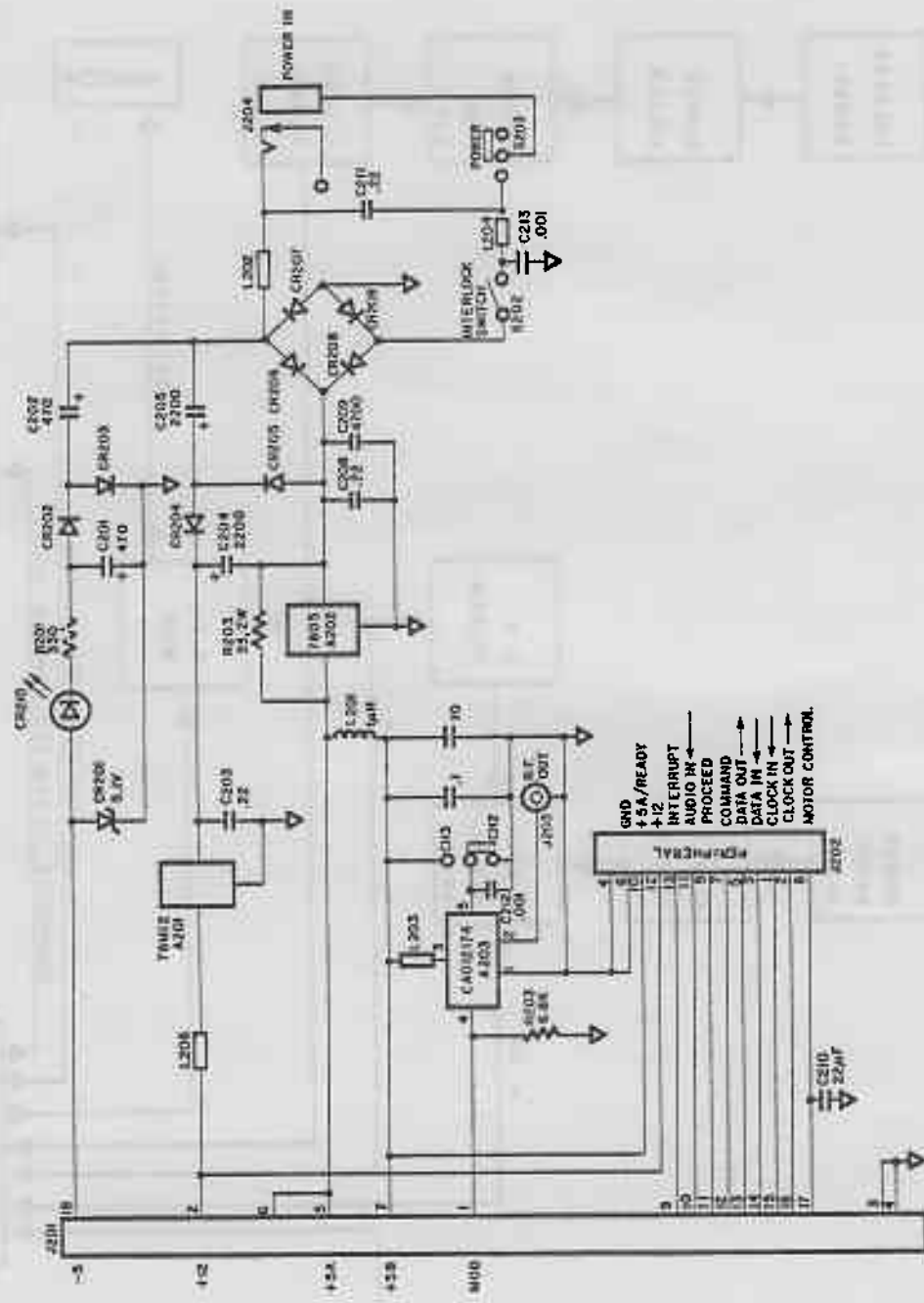


10 PAGE 2

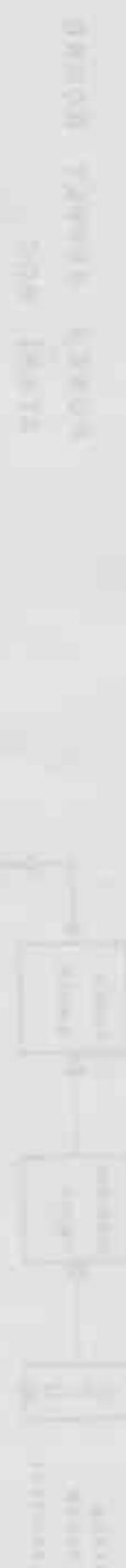
POWER SUPPLY BOARD ATARI 400



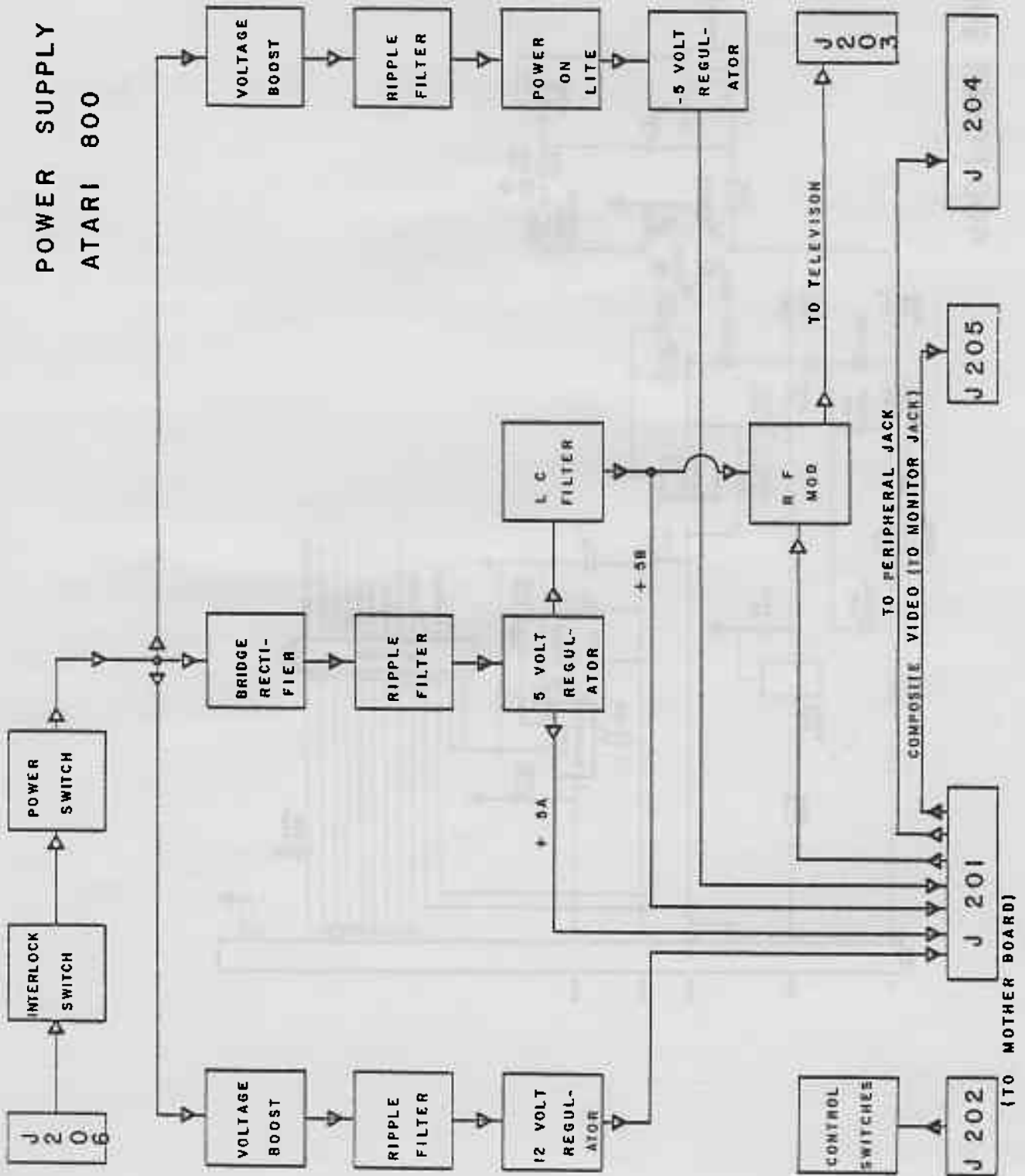
400 POWER SUPPLY



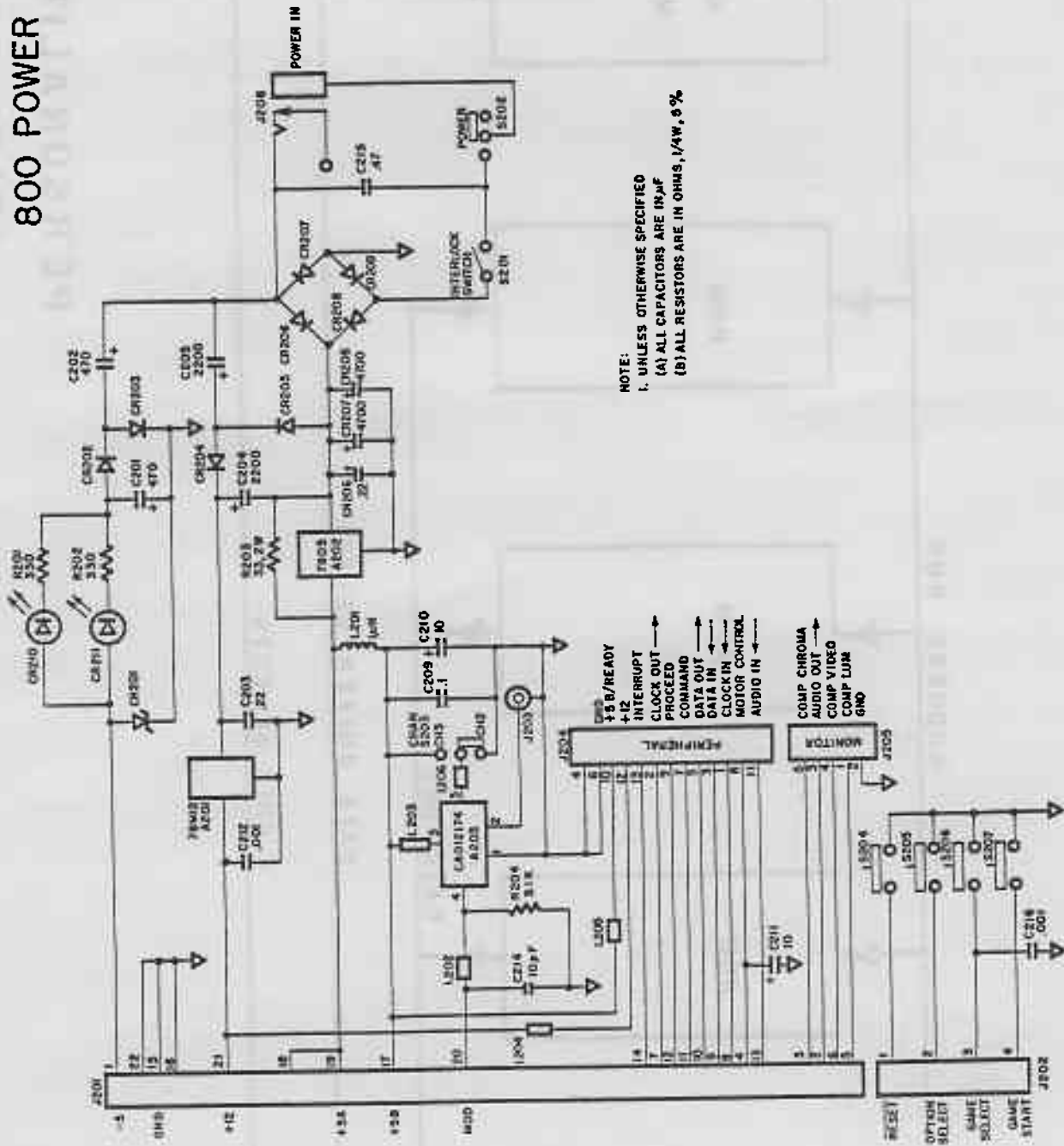
- GROUND
- +5A/READY
- +12
- INTERRUPT
- AUDIO IN
- PROCEED
- COMMAND
- DATA OUT
- DATA IN
- CLOCK IN
- CLOCK OUT
- MOTOR CONTROL



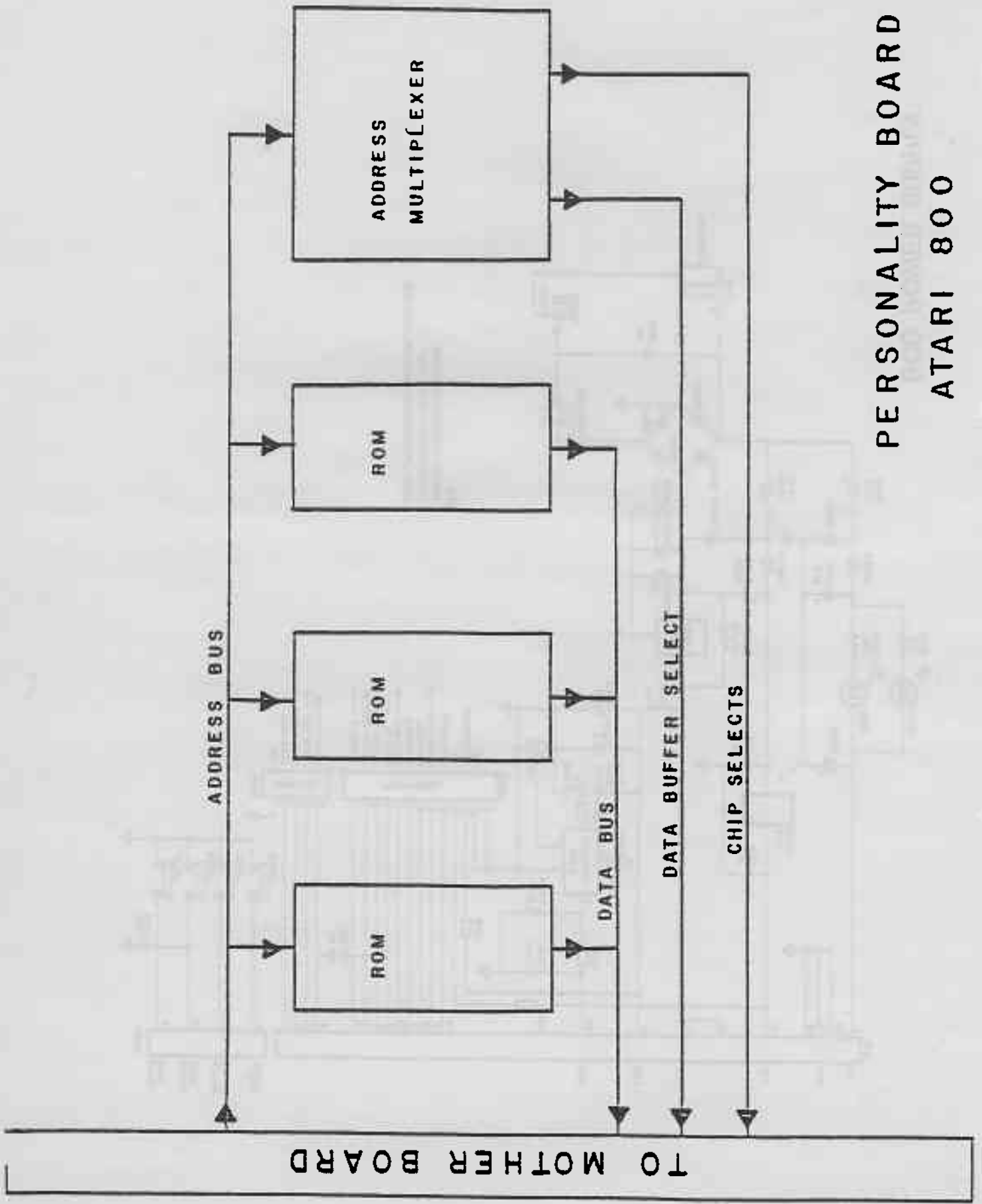
POWER SUPPLY BOARD ATARI 800



800 POWER SUPPLY

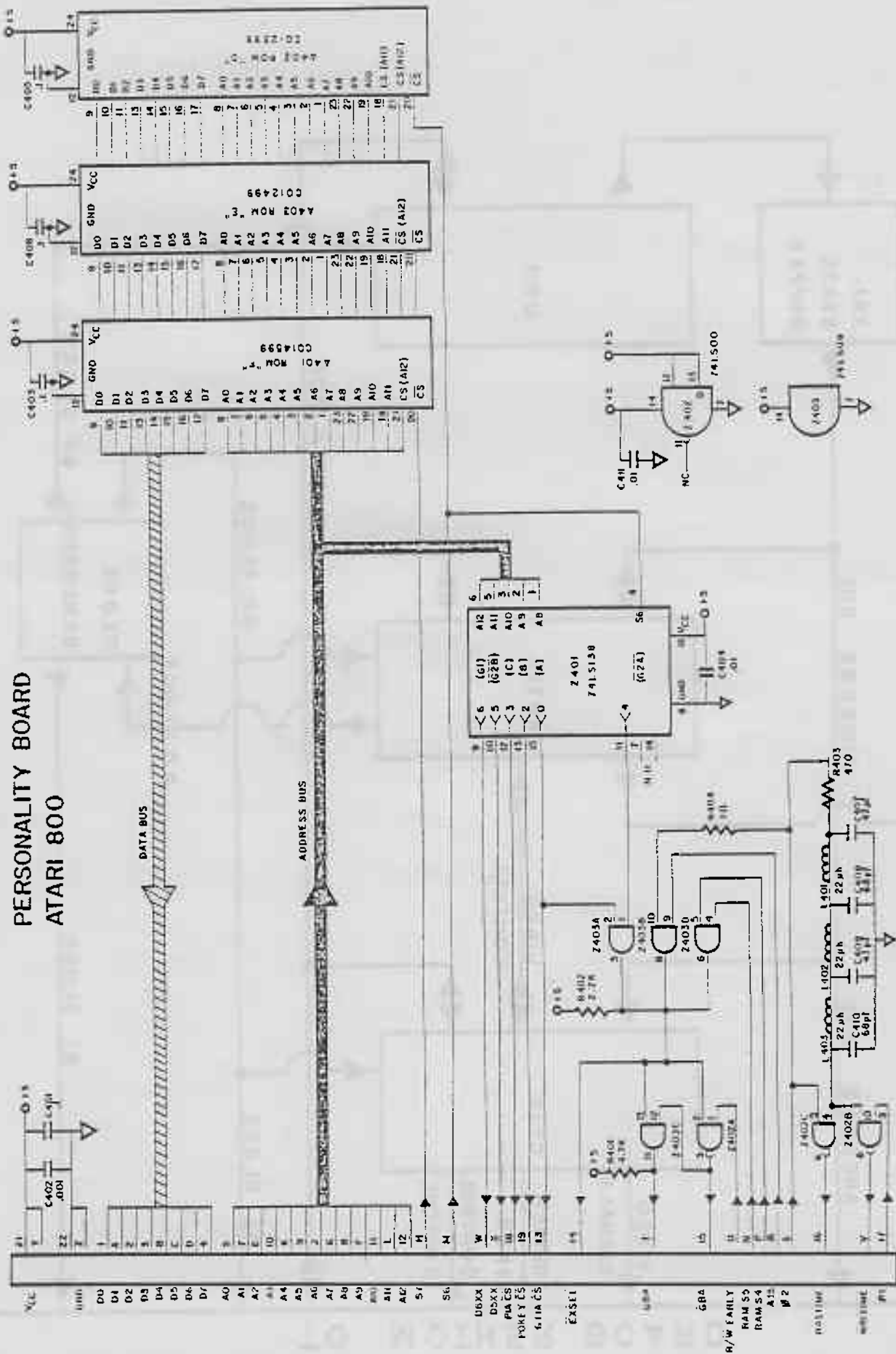


NOTE:
 1. UNLESS OTHERWISE SPECIFIED
 (A) ALL CAPACITORS ARE IN μ F
 (B) ALL RESISTORS ARE IN OHMS, 1/4W, 5%

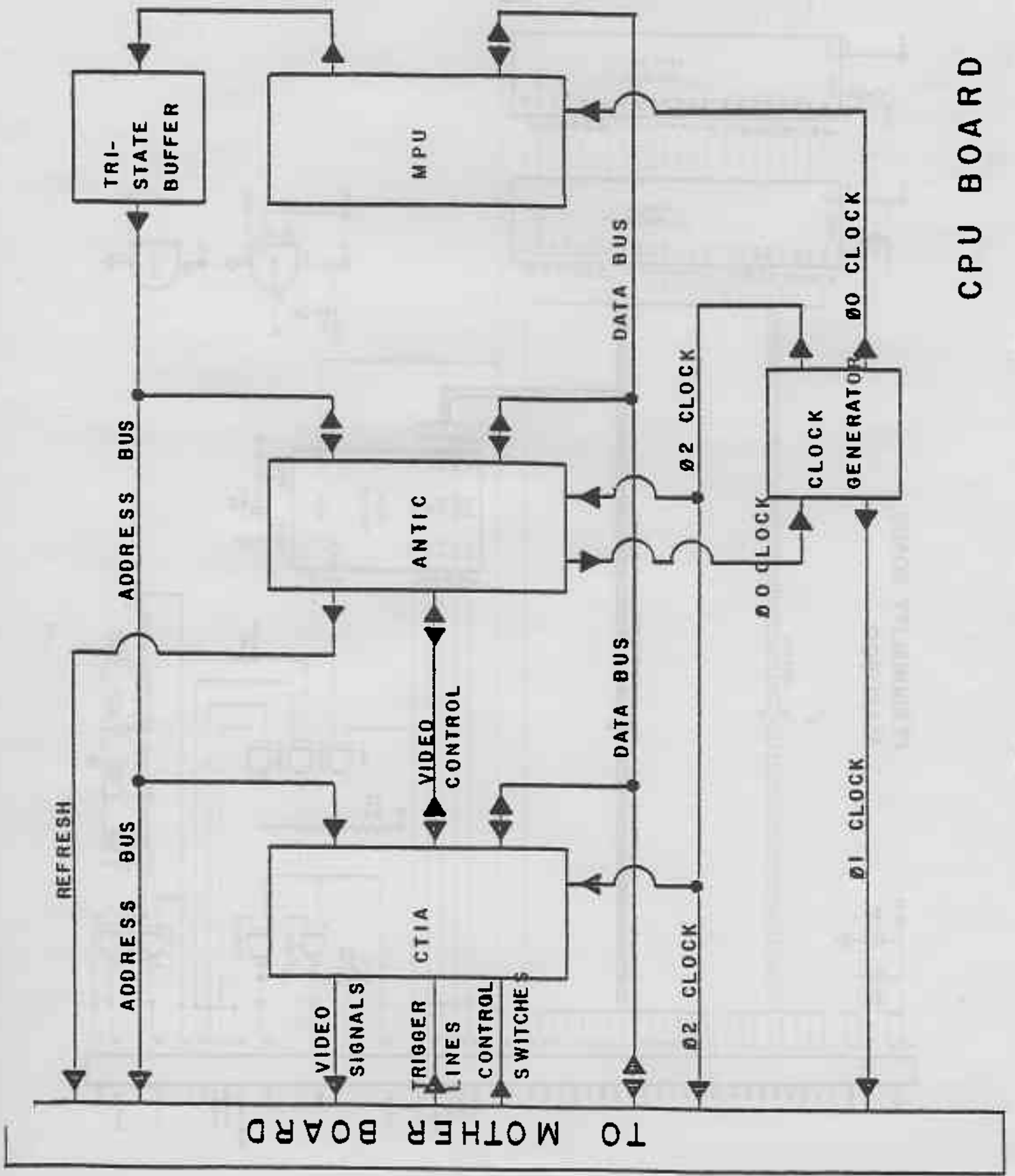


PERSONALITY BOARD
ATARI 800

PERSONALITY BOARD ATARI 800

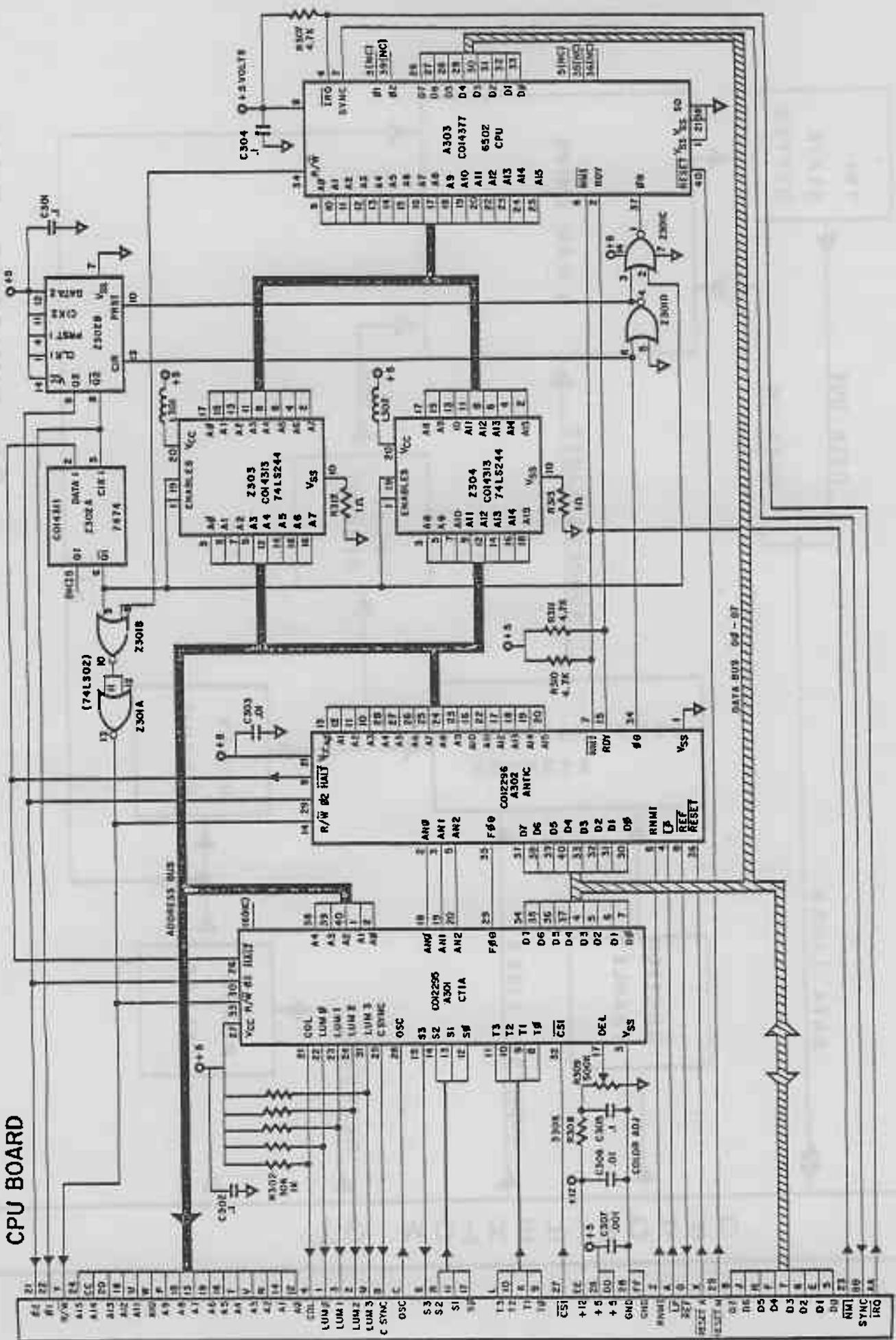


- VCC
- GND
- D0
- D1
- D2
- D3
- D4
- D5
- D6
- D7
- A0
- A1
- A2
- A3
- A4
- A5
- A6
- A7
- A8
- A9
- A10
- A11
- A12
- S1
- S6
- WE
- OE
- PIA CS
- POKEY CS
- 611A CS
- EXSEL
- UBA
- GBA
- R/W EARLY
- RAM S0
- RAM S4
- A15
- # 2
- POSITIVE
- NEGATIVE
- PT

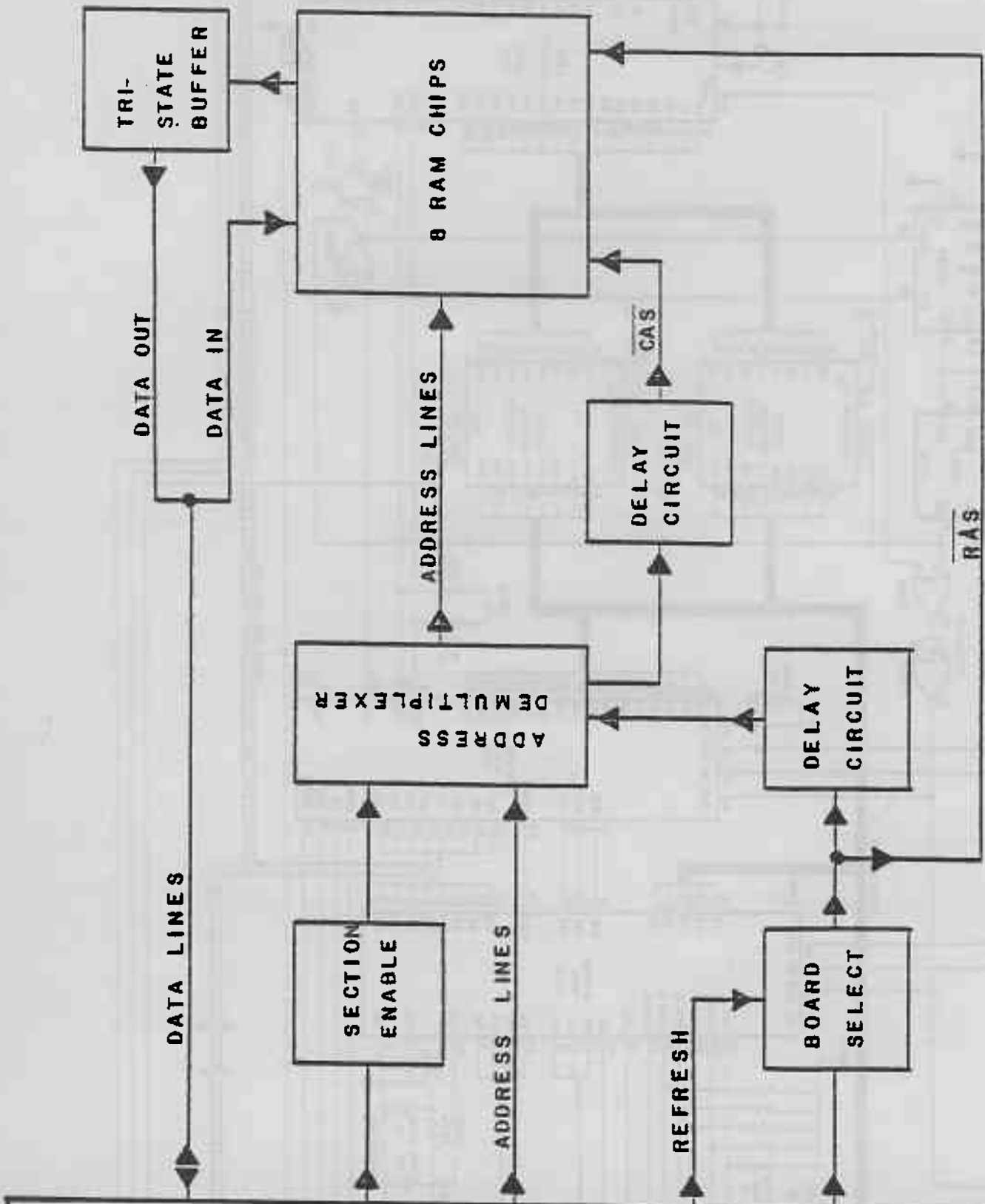


CPU BOARD

CPU BOARD

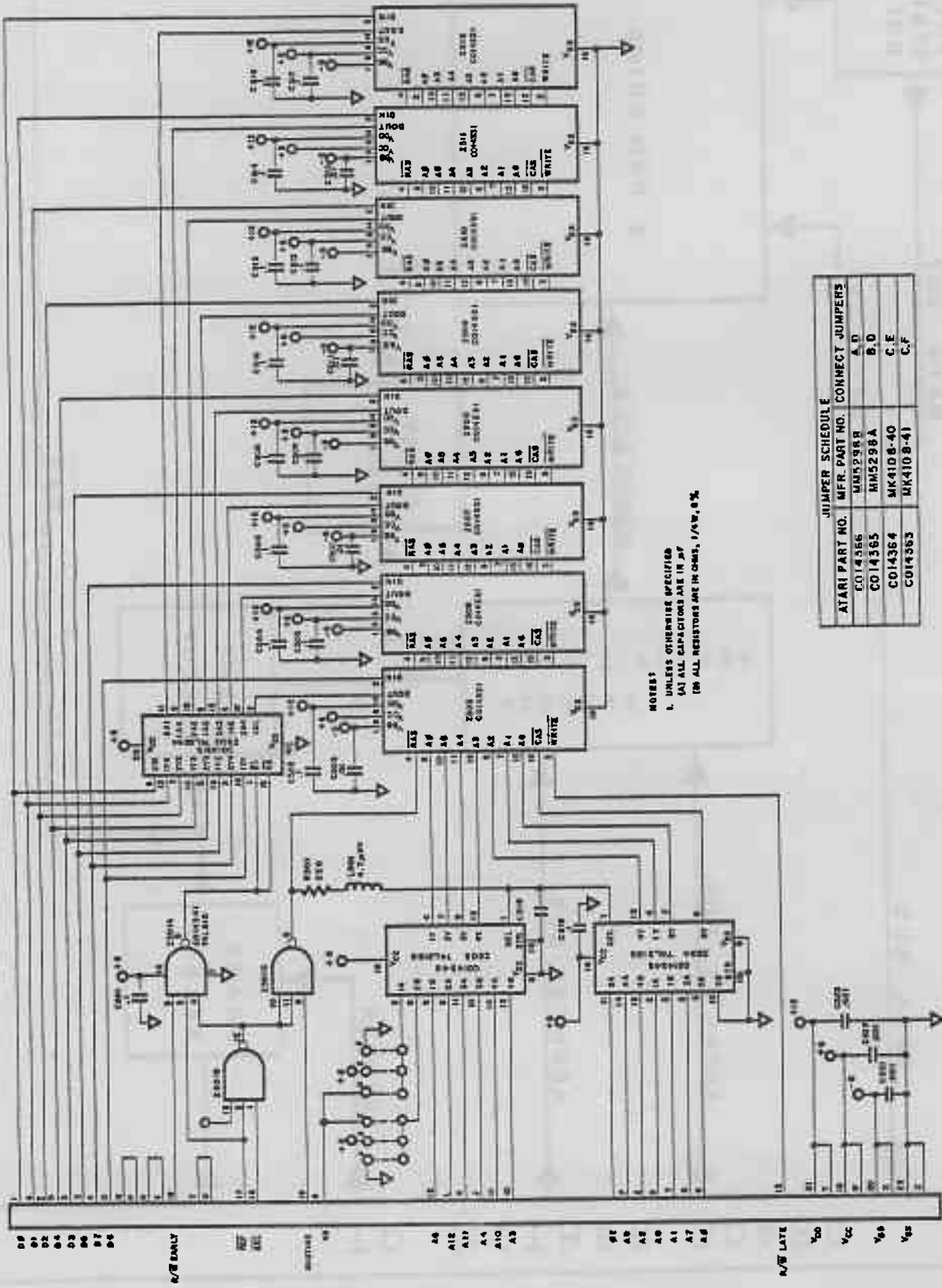


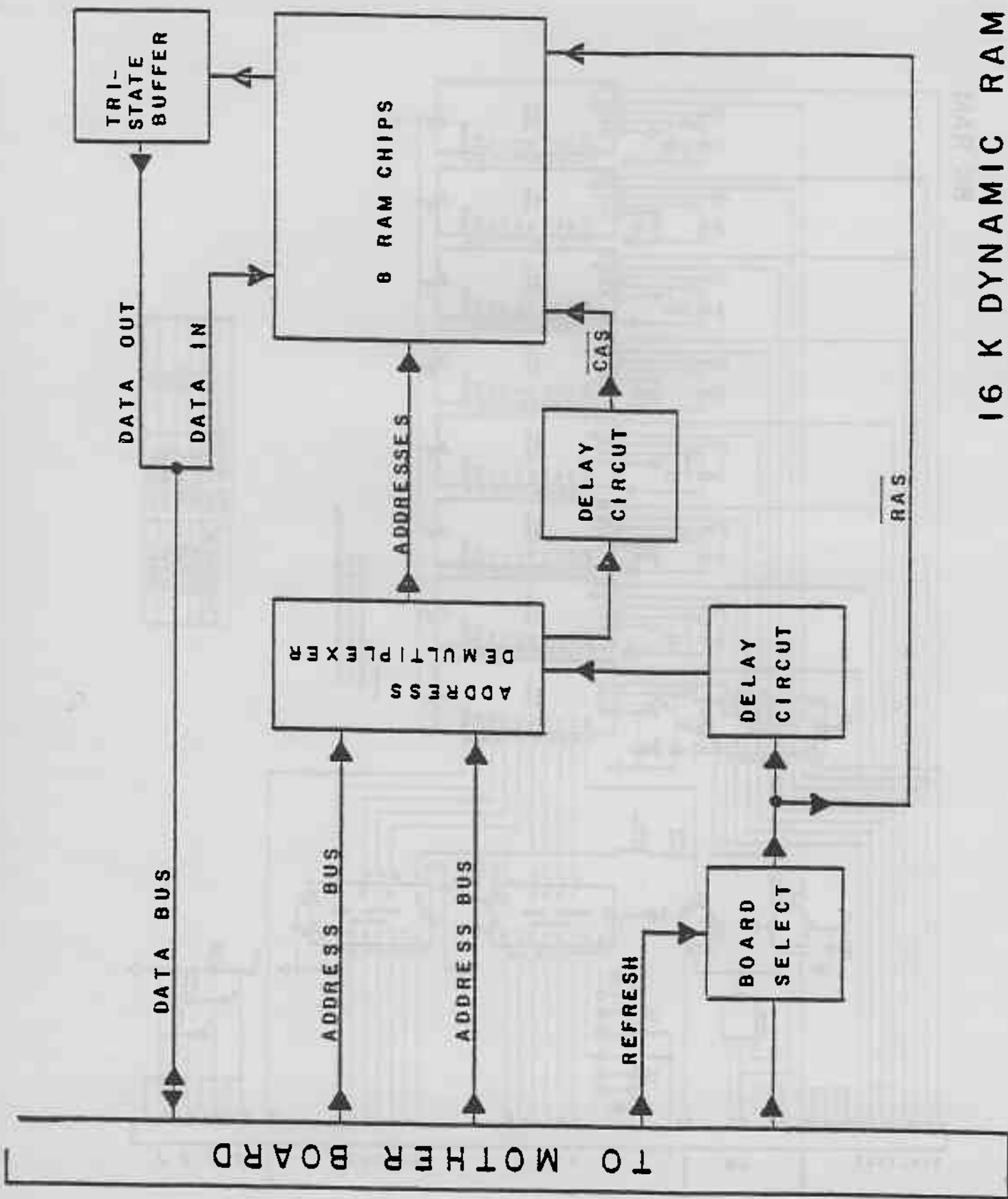
TO MOTHER BOARD



8K DYNAMIC RAM
ATARI

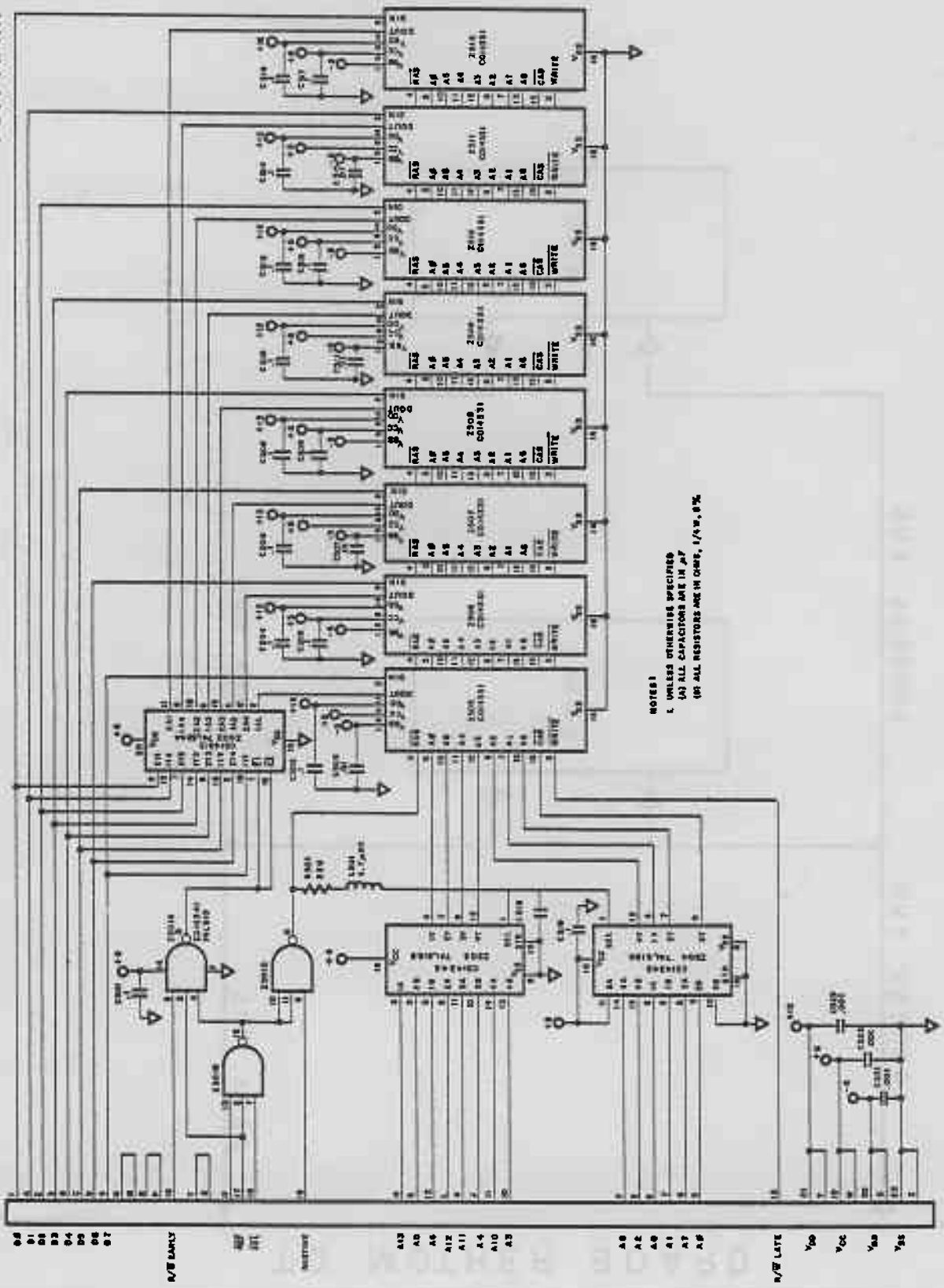
8K RAM



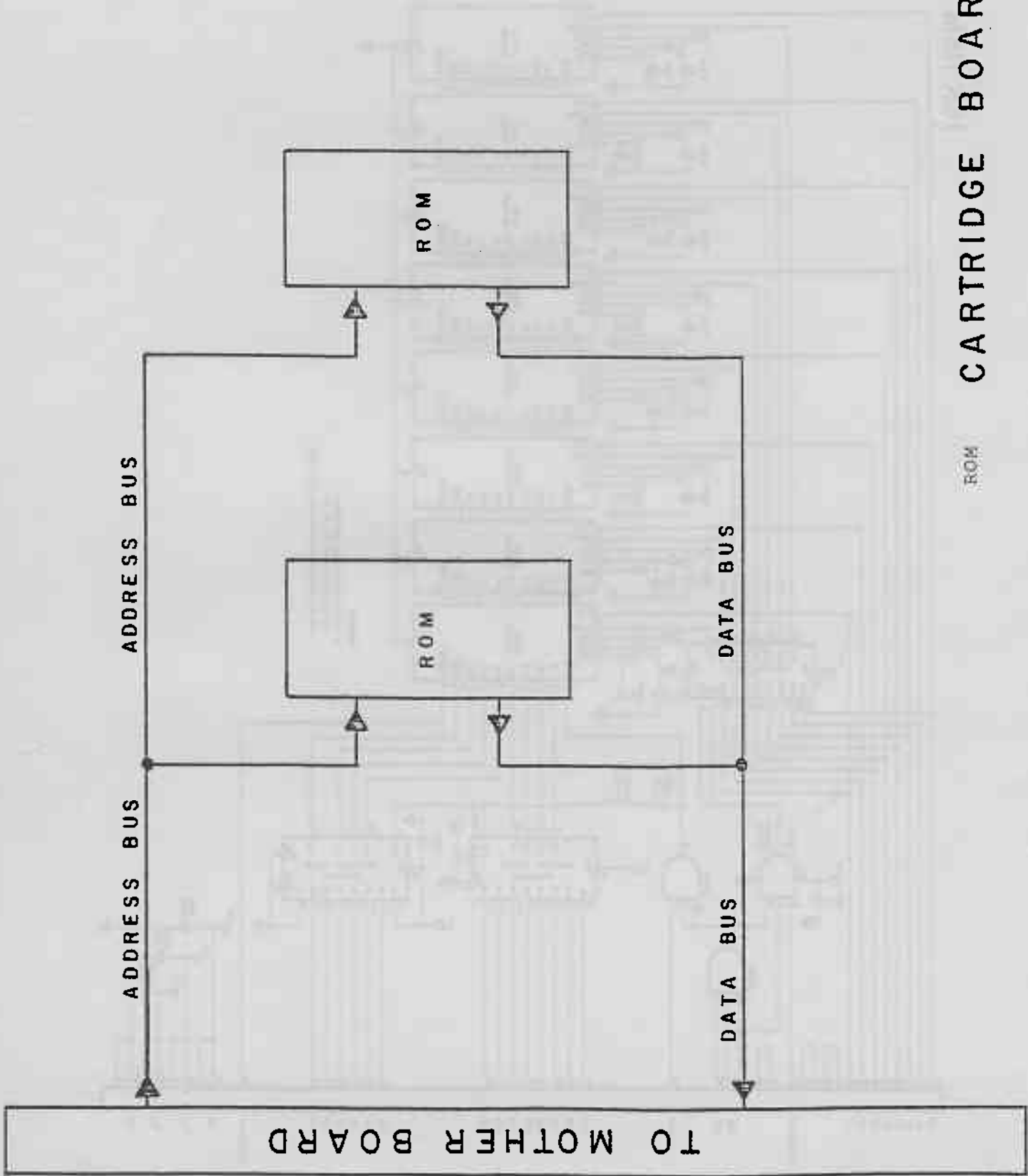


16 K DYNAMIC RAM
ATARI

16K RAM

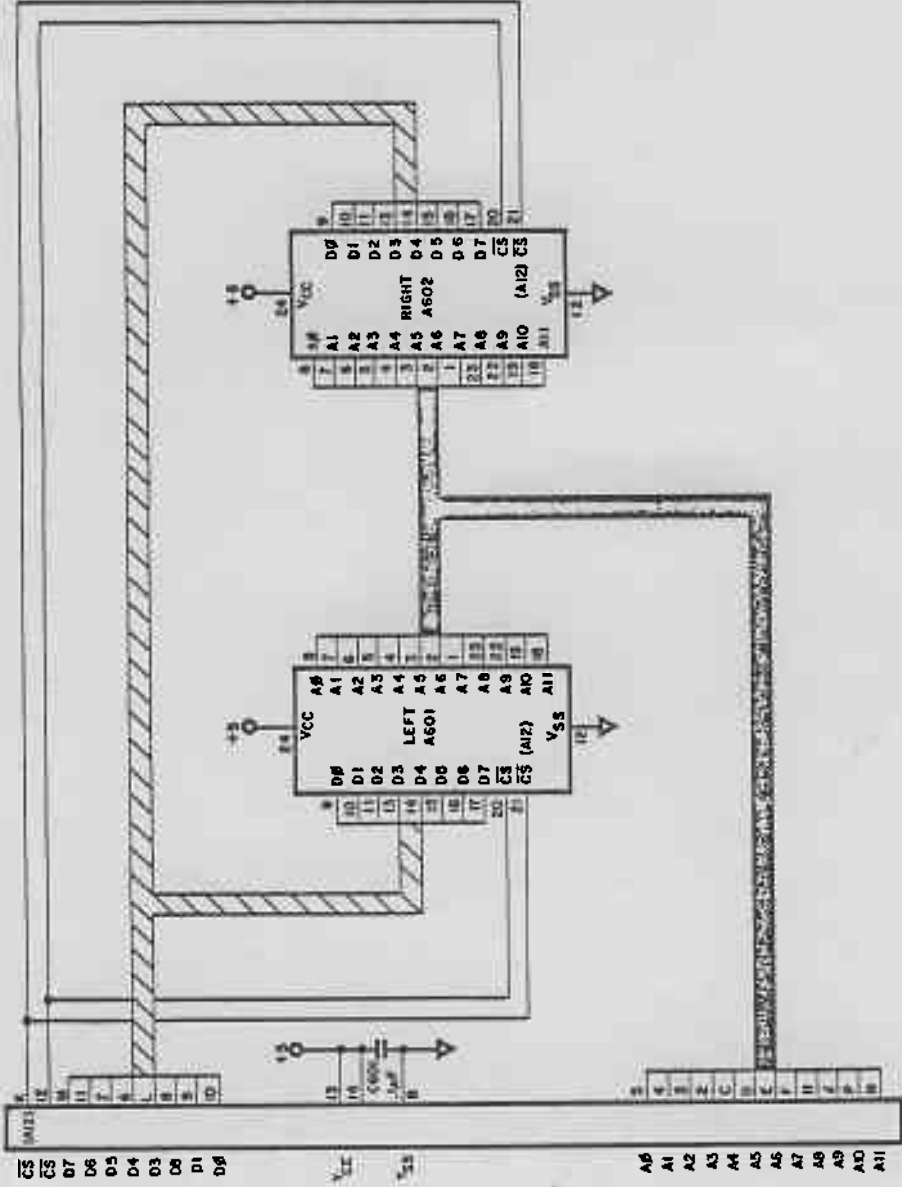


NOTES:
 1. UNLESS OTHERWISE SPECIFIED
 (A) ALL CAPACITORS ARE IN pF
 (B) ALL RESISTORS ARE IN OHMS, 1/4W, 5%



ROM CARTRIDGE BOARD

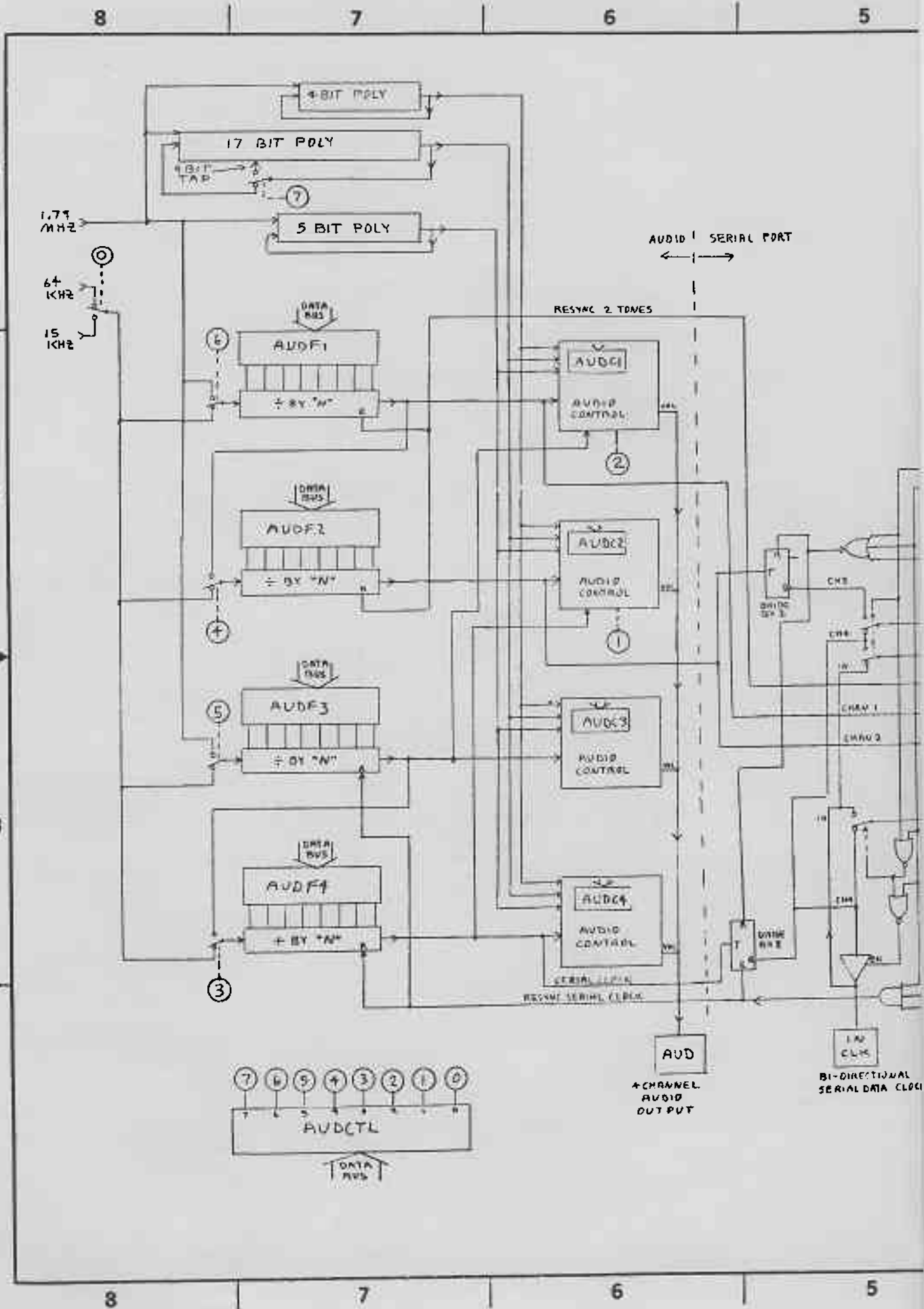
SCHEMATIC ROM CARTRIDGE

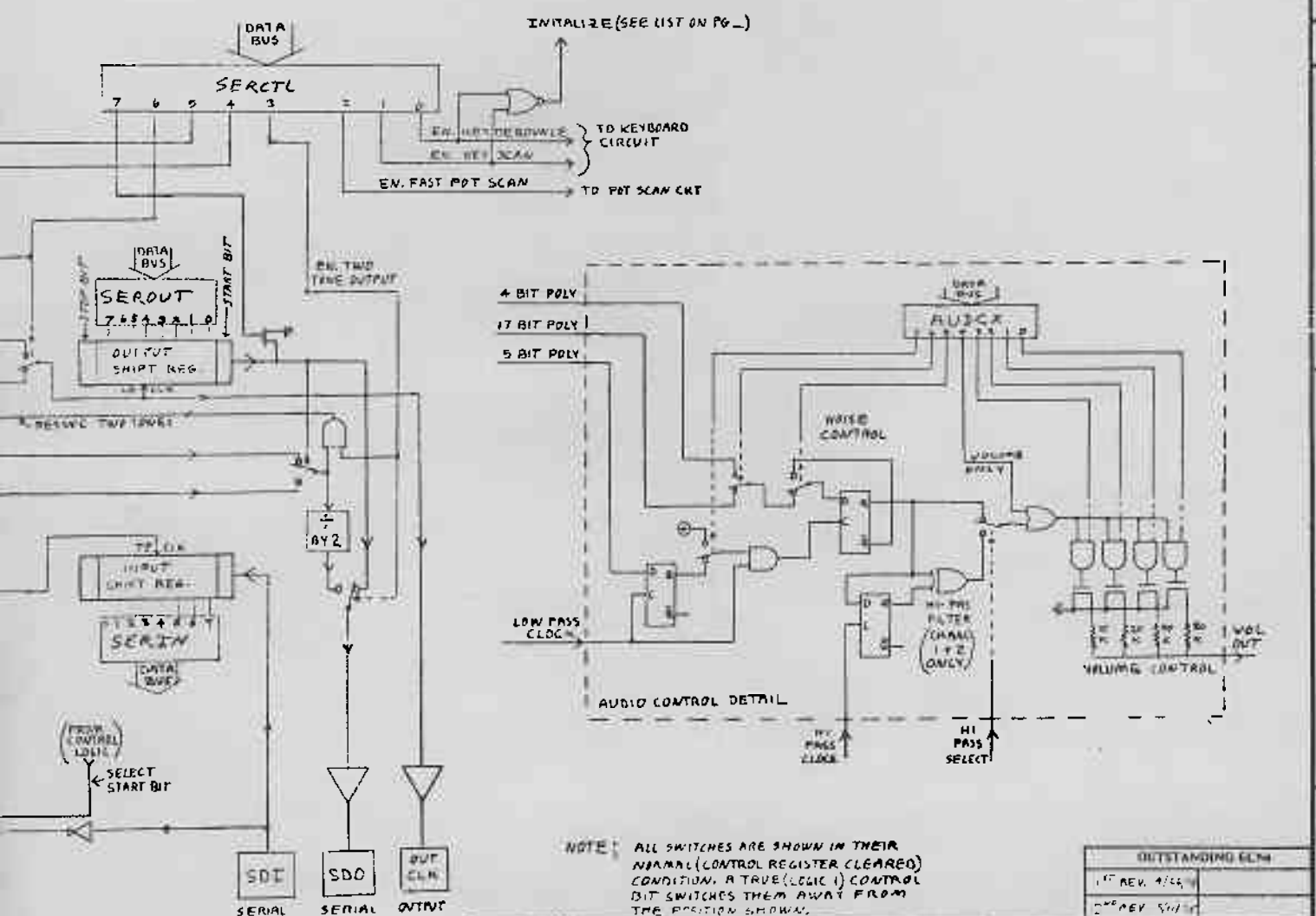


CS CS D7 D6 D5 D4 D3 D2 D1 D0

V_{CC} V_{SS}

A8 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11





NOTE: ALL SWITCHES ARE SHOWN IN THEIR NORMAL (CONTROL REGISTER CLEARED) CONDITION. A TRUE (LOGIC 1) CONTROL BIT SWITCHES THEM AWAY FROM THE POSITION SHOWN.

OUTSTANDING CLM	
REV. 1	DATE
REV. 2	DATE

	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: ANGLES ±.1° .5° ± .1 .125 ± .01 SURFACE FINISH ✓ .000 ± .001	DO NOT SCALE DRAWING DESIGNED BY: [] DATE: [] CHECKED BY: [] DATE: [] DRAWN BY: [] DATE: [] PROJECT ENGINEER: [] ALL DIMENSIONS: []	<p>Atari, Inc. 1265 Borregas Avenue Sunnyvale, Calif 94086</p> <p>ATARI® A Division of Commodore International Company</p>
TITLE COLLEEN MANUAL AUDIO AND SERIAL PORT BLOCK DIAGRAM			A

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APPENDIX A
USE OF PLAYER/MISSILE GRAPHICS
WITH BASIC

The ATARI® 400/800™ Hardware Manual should be read first to understand the details of the Player/Missile Graphics.

To enable the P/M Graphics from BASIC the following procedure can be used:*

1. Generate the playfield, either with a GRAPHICS call or build a custom display list with a series of POKE statements.
2. Enable P/M DMA control by a POKE 559 with either a 62 for single line resolution players or a 46 for double line resolution players.
3. There are four players and four missiles (or five players if the four missiles are combined into one player). Each of these has a horizontal position register that controls its horizontal position on the screen. The registers and their locations are as follows:

ADDRESS	HORIZONTAL POSITION OF
53248	Player 0
53249	Player 1
53250	Player 2
53251	Player 3
53252	Missile 1
53253	Missile 2
53254	Missile 3
53255	Missile 4

The horizontal positions can range on the playfield between 41 and 200. So POKE 53249,120 will move Player 1 to the middle of the screen.

*NOTE: All number references are decimal.

Use of Player/Missile Graphics
with BASIC, cont.

4. Each player (and its missile) has a color register which determines its color. These registers can be controlled by poking to the following locations:

ADDRESS	COLOR OF
704	P/M 0
705	P/M 1
706	P/M 2
707	P/M 3
711	fifth player (if enabled)

Thus a POKE 706,200 will color player 2 green.

5. The P/M bit information (those bytes which actually describe the shape of the player) must be stored in an area where it will not interfere with BASIC or the operating system. It must also start at a 2K memory boundary if single line resolution players are used, or a 1K boundary for double line resolution players.
6. The page number (i.e. number of 256 byte sections of memory) for the starting address of the P/M information obtained in step 5 is poked into location 54279.
7. Enable the P/M DMA by a POKE 53277,3.
8. The starting address of each player is obtained by multiplying the number obtained in step 6 by 256 and then adding the offset indicated in P/M memory configuration table.
9. The vertical position of the player is determined by its location in memory. After the initial offset is obtained in step 8, its height may be defined. Its range on the playfield is from 32 to 223 in single line resolution and from 16 to 111 in double line resolution. By adding the desired height to the initial offset, the absolute address of each player is found. The appropriate bit information for the player can now be poked into this address.

Use of Player/Missile Graphics
with BASIC, cont.

(9, cont.)

Example to Generate a rectangular box player, eight color
clocks wide and four lines high in immediate mode.

STEP	TYPE	RESULT
1	GRAPHICS 8	Setup Mode 8 Playfield
2	POKE 559, 62	Enable P/M DMA single line
3	POKE 53248,120	Set horizontal position
4	POKE 704,88	Set color to pink
5	I = PEEK(106)-8	Get P/M base address
6	POKE 54279,I	Store in base register
7	POKE 53277,3	Enable P/M DMA
8	J = I * 256 + 1024	Get player starting address
9	POKE J + 125,255 POKE J + 126,129 POKE J + 127,129 POKE J + 128,255	Draw player on screen.

Use of Player/Missile Graphics
with BASIC, cont.

DMACTL
bit D4=0

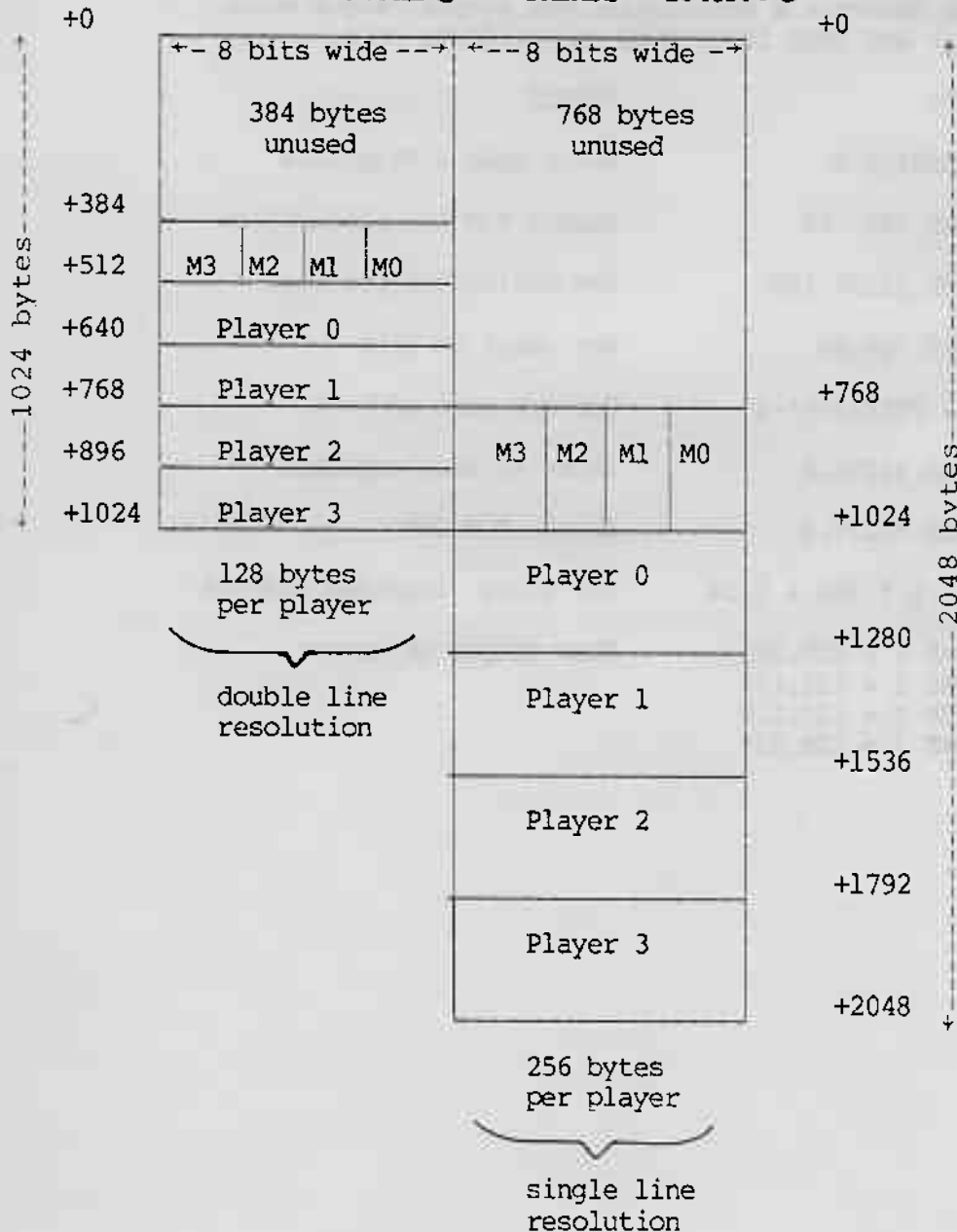
DMACTL
bit D4=1

PLAYER-MISSILE

Memory
Configuration

start at
PMBASE*1024256

start at
PMBASE * 2048256



Absolute address
determined by
PMBASE.

Relative address
shown along sides
of maps.

Each Player-Missile
section (128 bytes
in single line, 256
bytes in double line)
maps directly onto
the total height of
TV screen.

APPENDIX B

MIXING GRAPHICS MODES

I. GENERAL

This procedure describes how to mix several graphic modes on the TV screen at the same time using BASIC commands. Each graphics mode has a different number of scan lines per "Mode Line" (one line of a graphics mode). The TV screen must consist of 192 scan lines, so when mixing modes, they must be combined in such a way as to get 192 scan lines. This is accomplished by modifying the Display List.

When a graphics mode is set on the computer, the O/S allocates RAM space for the graphics mode, then builds the display list adjacent to the graphics RAM, and sets a pointer to the beginning of the display list. Each "mode line" is constructed from a "mode byte" in the display list that determines how many scan lines in each mode line. The display list describes the screen display from top to bottom.

A Display List must be built for the "max RAM mode" (the graphics mode that requires the most RAM) then modified with POKES to mix the other modes with it. This "max RAM mode" cannot be a split screen mode (text window), therefore "max RAM mode" +16 must be used. If the max RAM mode will be at the top of the screen, then the "LMS byte" (load memory scan byte) at the top of the Display List will already be correct. If not, the "LMS byte" will have to be modified.

The Display List is modified by POKING a new mode byte for each mode line that is not a max RAM mode line. At the end of the display list is a JUMP instruction pointing to the top of the Display list. When the Display List is modified, the JUMP instruction must be placed immediately after the last mode byte.

Example #1 will be used throughout this procedure to illustrate each step.

NORMAL

TV SCREEN

MODIFIED

96 x 2 = 192

MODE 7
96 LINES

192
SCAN
LINES

MODE 1
6 LINES

6 x 8 = 48

MODE 7
56 LINES

56 x 2 = 112

MODE 2
2 LINES

2 x 16 = 32

TOTAL = 192

TOTAL = 192

MODE 7
DISPLAY
LIST

MODE LINE #	(HEX)	DEC
1	(40)	77
—	LO	
—	HI	
2	(00)	13
3	(00)	13
4	(00)	13
~		
94	(00)	13
95	(00)	13
96	(00)	13
JUMP →	(41)	65
	LO	
	HI	

MODE 7
96 LINES

SCAN
LINE #

2 ← (LMS BYTE) → 1

— ← "START" → —

—

4

6

8

~

188

190

192

MODE 1
6 LINES

MODE 7
56 LINES

MODE 2
2 LINES

MODE
LINE #

1

—

—

2

3

4

5

6

7

8

~

~

61

62

63

64

JUMP →

MODIFIED
MODE 7
DISPLAY
LIST

MODE LINE #	(HEX)	DEC	SCAN LINE #
1	(46)	70	8
—	LO		—
—	HI		—
2	(06)	6	16
3	(06)	6	24
4	(06)	6	32
5	(06)	6	40
6	(06)	6	48
7	(00)	13	50
8	(00)	13	52
~			
61	(00)	13	158
62	(00)	13	160
63	(07)	7	176
64	(07)	7	192
JUMP →	(41)	65	
	LO		
	HI		
X			

EXAMPLE #1

Mixing Graphics Modes, cont.

II. PROCEDURE TO SET UP SCREEN IN MIXED MODES:

1. Select modes desired, then look up which mode is the max RAM mode from table #2.

example: modes selected - mode 1, mode 7, mode 2

mode 7 = max RAM mode

2. Use table #1 to calculate the number of mode lines such that the total number of scan lines = 192.

example:

mode	# mode line	scan lines per mode line	scan lines
1	6	8	48
7	56	2	112
2	2	16	32
			192 TOTAL

3. If the max RAM mode is at the top of the screen, then skip this step: Calculate the LMS byte by setting the left nibble to 4, then use table #1 to find the right nibble for the graphics mode at the top of the screen.

example: 1. left nibble = 4
 2. right nibble for mode 1 = 6
 3. LMS byte = 46 (HEX)

4. Calculate the mode byte for each mode. Set the left nibble to 0, use table #1 to find the right nibble for each mode.

example:

Mode	Left Nibble	Right Nibble	Mode Byte (HEX)
1	0	6	06
7	0	D	0D
2	0	7	07

Mixing Graphics Modes, cont.

II. PROCEDURE TO SET UP SCREEN IN MIXED MODES, cont.:

5. Convert all bytes to decimal.

example:

	Byte	(HEX)	DEC
	LMS	46	70
Mode 1		06	6
Mode 7		0D	13
Mode 2		07	7

6. Execute a graphics call on the computer using the max RAM mode (+16).

example: GRAPHICS 7 + 16

7. PEEK the Display List pointer and use it to calculate a variable labelled "START".

example: START = PEEK(560) + PEEK(561) * 256 + 4

8. If the max RAM mode is at the top of the screen, then skip this step: Poke the LMS byte to location START-1.

example: POKE START-1,70

9. Every mode line requires a mode byte in the Display List in the same order as the mode lines appear on the screen. The mode bytes must be POKED into the Display List at location START + offset, where offset = mode line #.

Example:

	<u>MODE LINE #</u>	<u>POKE INSTRUCTION</u>
	2	POKE START + 2,6
	3	POKE START + 3,6
MODE 1	4	POKE START + 4,6
	5	POKE START + 5,6
	6	POKE START + 6,6
MODE 7	see note for mode 7 (max RAM mode)	
MODE 2	63	POKE START + 63,7
	64	POKE START + 64,7

NOTE: The Display List will already be correct for the max RAM mode, therefore its mode bytes do not need to be POKED.

III. PROCEDURE TO PRINT AND PLOT IN MIXED MODES, cont.

2. Some modes may have mode line #'s outside of their normal range.

example: Mode 2 normally has mode line #'s 1 through 12 (full screen). These are modified to #63 and #64 in example #1.

To prevent the computer from giving a "cursor out of range" error message the following procedure can be used:

- a. Set a variable labelled "MEMST" to be the display memory start pointer.
 $MEMST = PEEK(START) + PEEK(START + 1) * 256$
- b. Set a variable labelled CHRPOS to position characters to be printed on the target line.

$$CHRPOS = MEMST + [(M_1 - 1) * R - M_2 * (R - 20) - M_3 * (R - 10)] + X$$

Where:

X = horizontal position of character on the target line.

R = the RAM per line of the Max RAM Mode (table #1).

M₁ = the Mode Line # of the target line.

M₂ = the number of mode lines of 20 bytes of RAM per line above the target line.

M₃ = the number of mode lines of 10 bytes of RAM per line above the target line.

Example: calculate CHRPOS for Mode Line #64 (the last line of the Mode 2 area) at horizontal position 5.

$$X = 5$$

$$R = 40$$

$$M_1 = 64$$

$$M_2 = 7 \text{ (6 from Mode 1 area, 1 from Mode 2 area).}$$

$$M_3 = 0$$

$$CHRPOS = MEMST + [(64 - 1) * 40 - 7 * (40 - 20) - 0 * (40 - 10)] + 5$$

$$CHRPOS = MEMST + [(63) * 40 - 7 * (20) - 0 * (30)] + 5$$

$$CHRPOS = MEMST + [2520 - 140] + 5$$

$$CHRPOS = MEMST + [2380] + 5$$

$$CHRPOS = MEMST + 2385$$

Mixing Graphics Modes, cont.

TABLE #1

REMARK	MODE BYTE		C.C. PER PIXEL	SCAN LINES PER MODE LINE	# COLORS	MODE	RAM PER LINE
	LEFT NIBBLE (HEX)	RIGHT NIBBLE (HEX)					
①	4	CHAR	2	8	15	0	40
			3	10	1½	-	40
			4	8	4	-	40
②	0	MODES	5	16	4	-	40
			6	8	5	1	20
			7	16	5	2	20
①	4	GRAPHIC	8	8	4	3	10
			9	4	2	4	10
			A	4	4	5	20
			B	2	2	6	20
			C	1	2	-	20
②	0	MODES	D	2	4	7	40
			E	1	4	-	40
			F	1	1½	8	40
BLANK	0-7	④	0	BLANK	-	-	-
JUMP	4	SPECIAL	1	JUMP	-	-	-

①. When the max RAM mode is not at the top of the screen, the left nibble of the LMS byte must be changed to a 4.

②. Left nibble for all mode bytes after the LMS byte.

③. Color & Lum for the field is controlled by Setcolor 2, and Lum for characters or graphics from Setcolor 1.

④. JUMP - used to end the display list and return to the beginning.

BLANK - to output selected number of background lines.

Mixing Graphics Modes, cont.

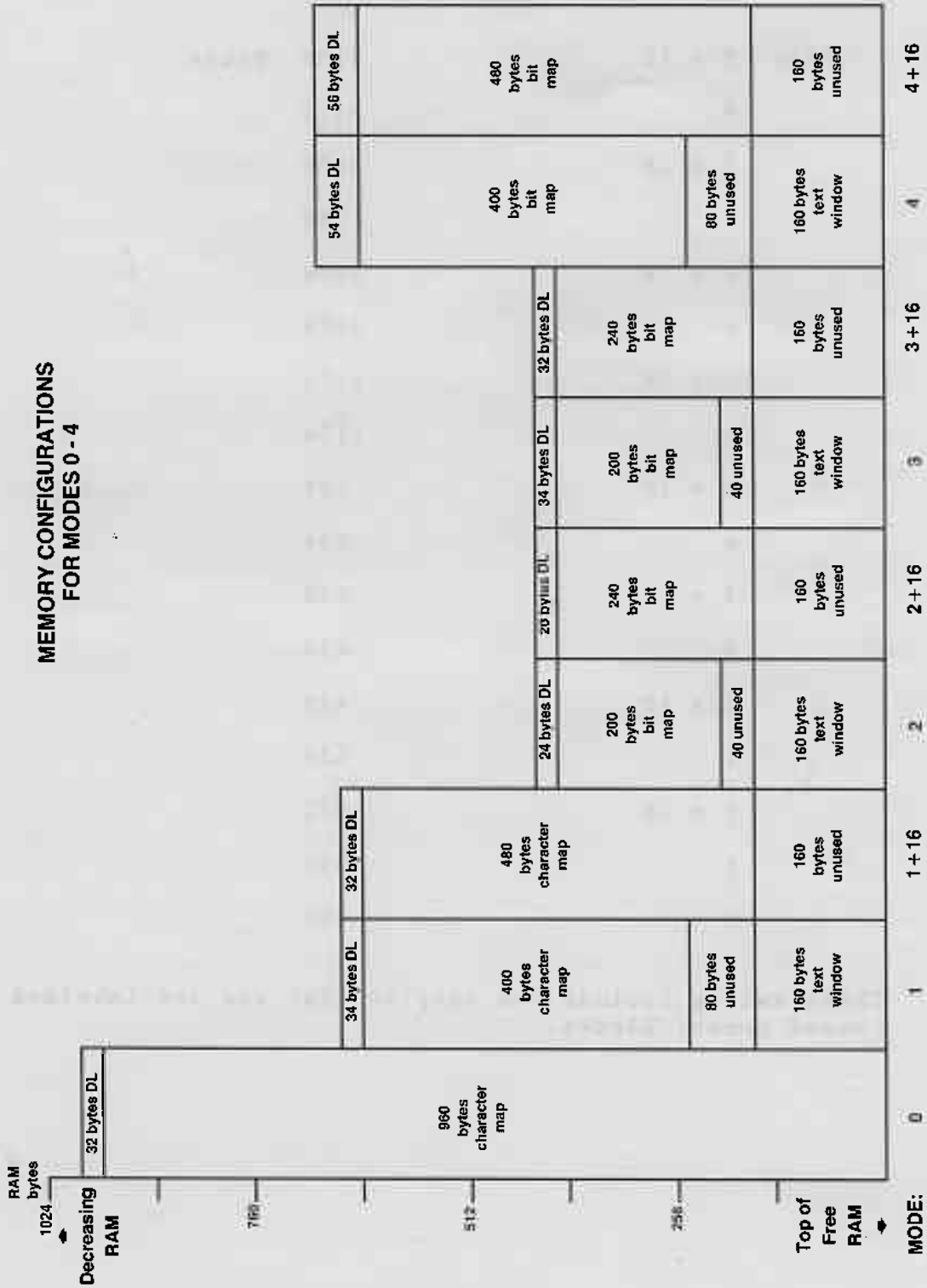
TABLE #2

GRAPHICS MODES
RAM REQUIREMENTS

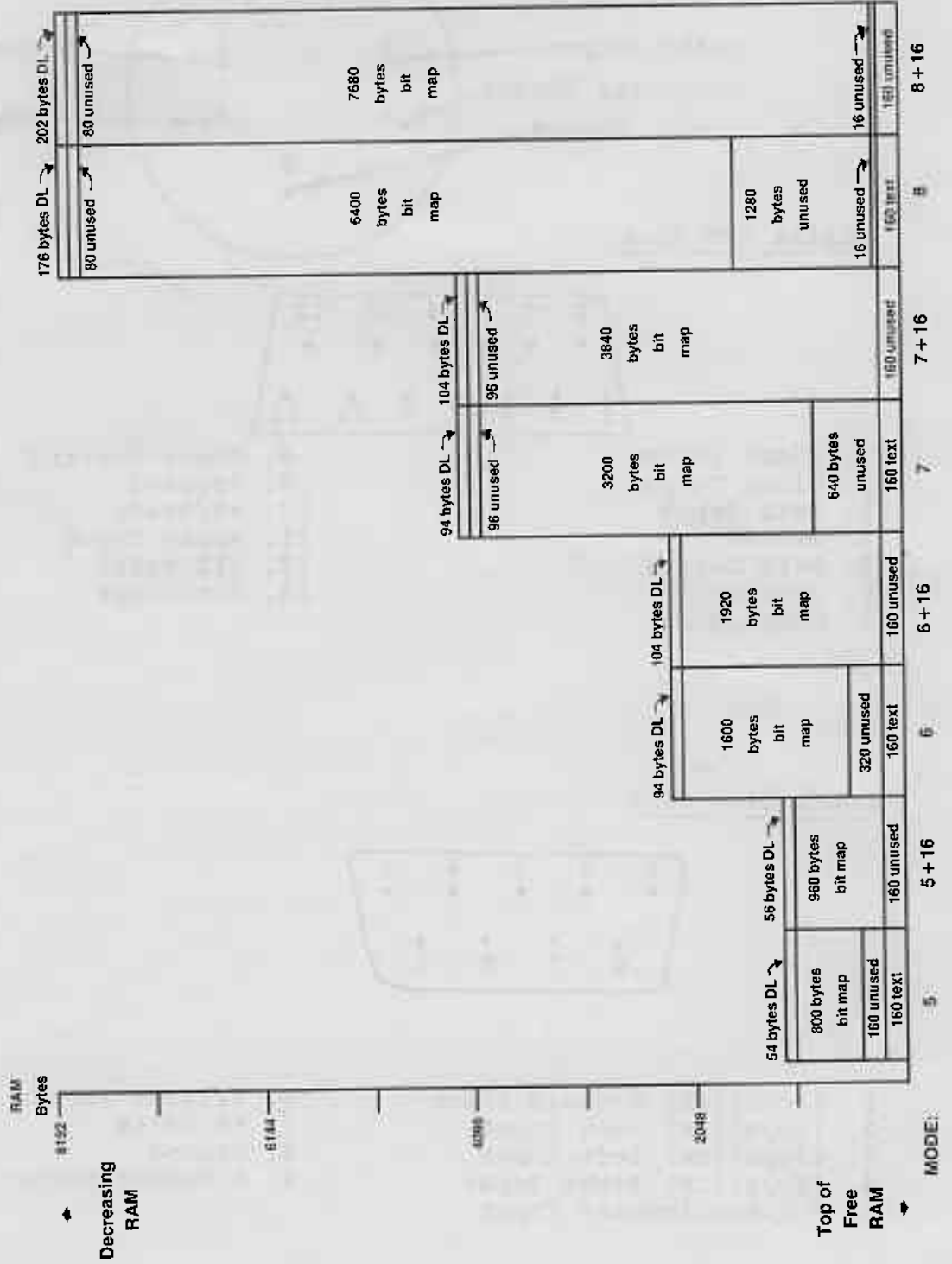
Mode	8 + 16	8138 Bytes
	8	8112
	7 + 16	4200
	7	4190
	6 + 16	2184
	6	2174
	5 + 16	1176
	5	1174
	4 + 16	696
	4	694
	3 + 16	432
	3	434
	2 + 16	420
	2	424
	1 + 16	672
	1	674
	0	992

These values include the display list and any imbedded unused memory blocks.

MEMORY CONFIGURATIONS FOR MODES 0 - 4



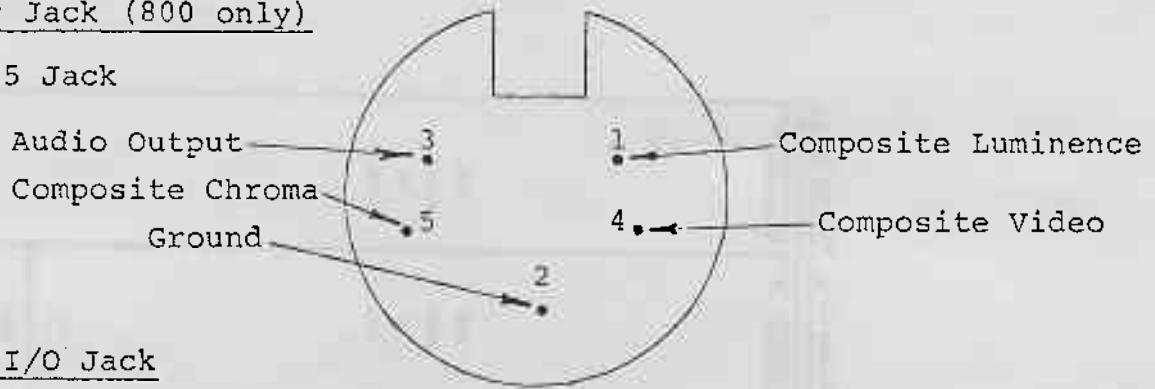
MEMORY CONFIGURATIONS FOR MODES 5 - 8



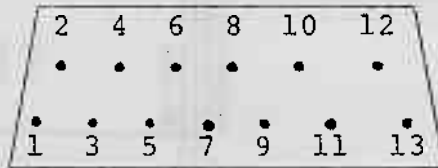
APPENDIX C: PINOUTS

Monitor Jack (800 only)

D.I.N. 5 Jack

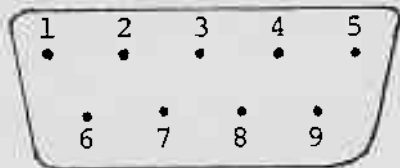


Serial I/O Jack



- | | |
|-----------------|------------------|
| 1. Clock Input | 8. Motor Control |
| 2. Clock Output | 9. Proceed |
| 3. Data Input | 10. +5/Ready |
| 4. Ground | 11. Audio Input |
| 5. Data Output | 12. +12 volts |
| 6. Ground | 13. Interrupt |
| 7. Command | |

Controller Jack



- | | |
|-----------------------------|--------------------------|
| 1. (Joystick) Forward Input | 6. Trigger Input |
| 2. (Joystick) Back Input | 7. +5 volts |
| 3. (Joystick) Left Input | 8. Ground |
| 4. (Joystick) Right Input | 9. A Potentiometer Input |
| 5. B Potentiometer Input | |